

DataSheet

10GBase SFP+ LR/LW Optical Transceivers

WST-SFP+LR-x



Applications:

- 10GBASE-LR 10Gigabit Ethernet
- High-speed storage area networks
- Computer cluster cross-connect
- Custom high-speed data pipes

Features:

- Optical interface compliant to IEEE 802.3ae
 10GBASE-LR/LW
- Compliant with SFP+ MSA
- Data Rate 10.3125 Gbps
- 1310nm DFB TOSA and PIN ROSA
- Applicable for 10 km SMF connection
- LC duplex receptacle
- Low power dissipation (<1W)</p>
- Hot Pluggable
- All-metal housing for superior EMI performance
- Built in digital diagnostic Functions
- Operating case temperature range: Commercial Temperature:0°C~70°C Extended Temperature:-5°C~85°C Industrial Temperature:-40°C~85°C
- RoHS Compliant

Description

WaveSplitter's WST-SFP+LR-x transceivers support the 2-wire serial communication protocol as defined in the SFP+ MSA.

The standard SFP serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.

Additionally, WST-SFP+LR-x transceivers provide a unique enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The SFP MSA defines a 256-byte memory map in EEPROM that is accessible over a 2-wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the SFP transceiver into those segments of the EEPROM that are not write-protected. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer.

The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Мах
Storage Temperature Range	Ts	°C	-40	+85
Power Supply Voltage	Vcc	V	0	+3.6
Relative Humidity	RH	%	5	95
Optical Receiver Power (Damage)		dBm		1.5

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Тур	Мах
Case Operating Temperature Range-CT	T _{c-CT}	°C	0	25	+70
Case Operating Temperature Range-ET	T _{c-ET}	°C	-5	25	+85
Case Operating Temperature Range-IT	T _{c-IT}	°C	-40	25	+85
Power Supply Voltage	V _{cc}	V	3.135	3.3	3.465
Power Supply Current	Icc	mA			300
Power Consumption		mW		800	1000
Data rate		Gbps		10.3125	

Specifications (tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min.	Тур.	Max.	Notes			
Electrical Characteristics									
Transmitter Differential Input Voltage	VIN	mV _{pp}	180		700				
Receiver Differential Output Voltage	Vo	mV _{pp}	300		850				
	V _{OH}	V	2		Vcc				
Loss of Signal (LOS)	Vol		Vee		Vee+0.8				
	Vih		2		Vcc				
Transmitter Disable (TX-Disable)	VIL	V	Vee		Vee+0.8				
Rx Output Rise and Fall Time	Tr/Tf	ps	28			20% to 80%			

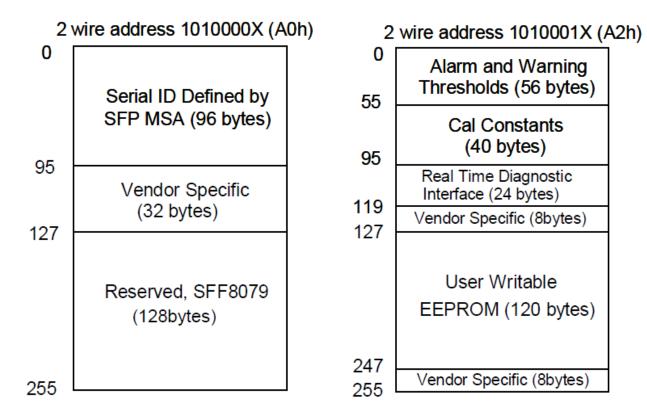
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Optical transmitter Characteristics									
Averag	e Launch Power	Po	dBm	-8.2		0.5			
Center	wavelength	λc	nm	1260		1355			
Side M	ode Suppression Ratio	SMSR	nm	30					
Extinct	ion ratio	Er	Db	3.5					
Transm	nitter and dispersion penalty(max)	TDP	dB			3.2			
Optical	power OMA	Рома	dBm	-5.2					
OMA-T	DP	Poma-tdp	dBm	-6.2					
Averag transm	e launch power of OFF itted	Poff	dBm			-30			
RIN ₁₂ C	MA	RIN	dB/Hz			-128			
Optical Return Loss Tolerance			dB	12					
Output	eye	Compliant with IEEE802.3ae eye mask							
		Optical re	eceiver Chara	cteristics					
Center	wavelength	λ_{c}	Nm	1260		1355			
Averag	e receiver power(max)	P _{max}	dBm			0.5			
Averag	e receiver power(min)	Pmin	dBm	-14.4					
Receiv	er Reflectance	R _{rx}	dB			-12			
Receiv	er Sensitivity in OMA		dBm			-12.6			
Stresse	ed Sensitivity in OMA		dBm			-10.3	1		
Vertical eye closure penalty			dB	2.2			2		
Stressed eye jitter			Ulp-p	0.3			1		
	Assert	LOSA	dBm	-30					
LOS	Deassert	LOSD	dBm			-12			
LOS H	ysteresis	LOSH	dB	0.5					

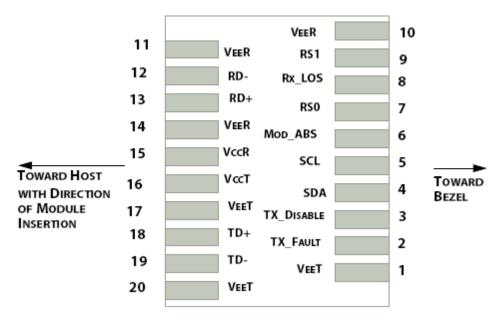
Note1. Receiver sensitivity is informative. Stressed receiver sensitivity shall be measured with conformance test signal for $BER = 1 \times 10^{-12}$.

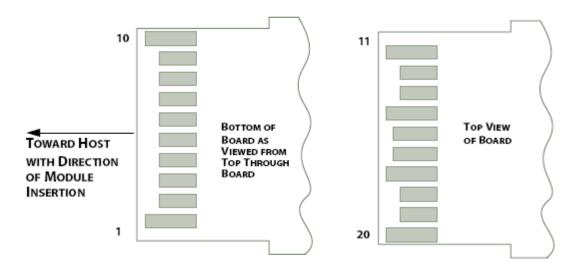
Note2. Vertical eye closure penalty and stressed eye jitter are the test conditions for measuring stressed receiver sensitivity. They are not the required characteristic of the receiver.

EEPROM Memory Map



Pin Definition





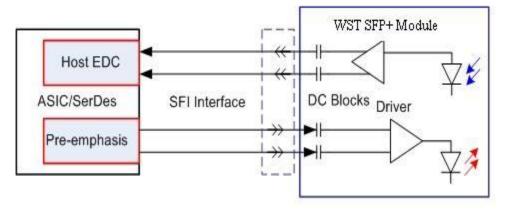
Module Electrical Pin Definition

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Disable	Transmitter Disable; Turns of transmitter laser output	3
4	LVTTL-I/O	SDA	2-wire Serial Interface Data Line (Same as MOD-DEF2 in the INF-8074i)	
5	LVTTL-I/O	SCL	2-wire Serial Interface Clock (Same as MOD-DEF1 in the INF-8074i)	
6		Mod_ABS	Module Absent, connected to VeeT or VeeR in the module	2
7	LVTTL-I	RS0	Rate Select 0, optionally controls SFP+ module receiver. When high input signaling rate> 4.25 GBd and when low input signal rate \leq 4.25 GBd.	
8	LVTTL-O	Rx_LOS	Receiver Loss of Signal Indication	2
9	LVTTL-I	RS1	Rate Select 1, optionally controls SFP+ module transmitter. When high input signaling rate> 4.25 GBd and when low input signal rate \leq 4.25 GBd.	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Non-Inverted Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Transmitter 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Receiver Non-Inverted Data Output	
19	CML-I	TD-	Receiver Inverted Data Output	
20		VeeT	Module Transmitter Ground	1

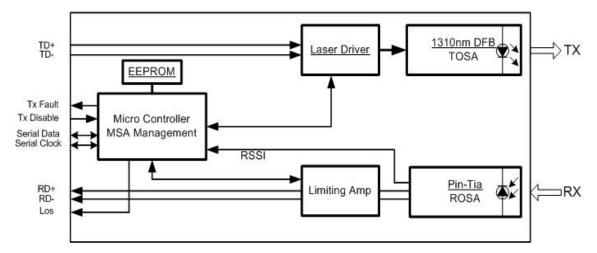
Note1: Module ground pins are isolated from the module case and chassis ground within the module.

Note2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board. **Note3:** Shall be pulled up with 4.7k to 10k ohm to VccT in the module.

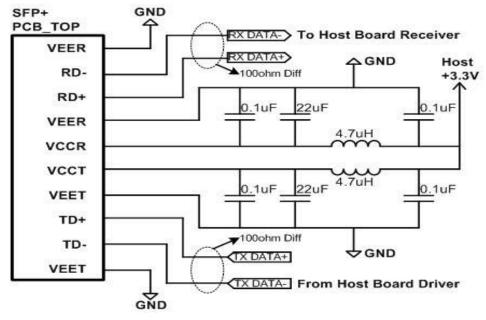
Application in System

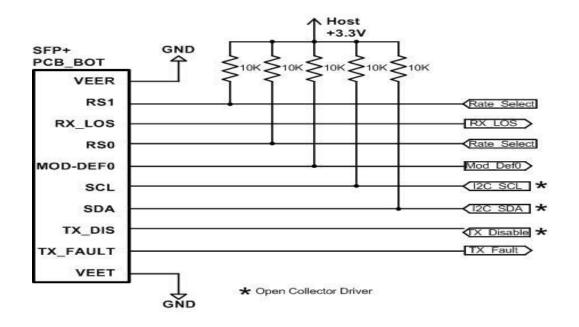


Block Diagram



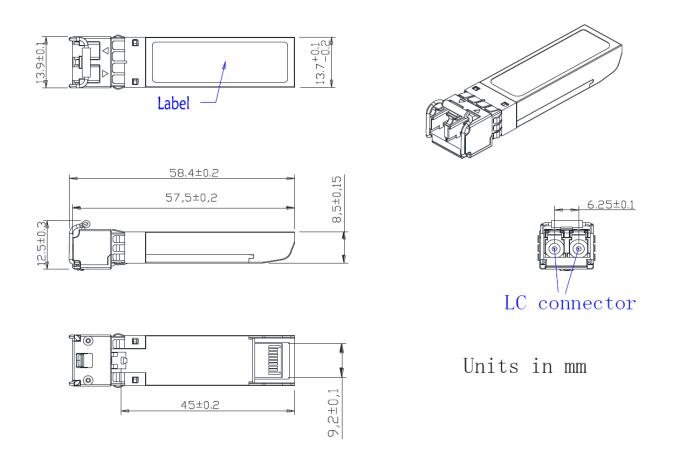
Typical Application Circuit





Mechanical

Comply to SFF-8432 rev. 5.0, the improved Pluggable form factor specification. Bail latch color is Blue for LR



Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Other	Application code
WST-SFP+LR-C	SFP+	10.31 Gbps	1310nm DFB	-8.2~ 0.5dBm	PIN	-12.6dBm	0~70°C	10km	DDM RoHS	10GBASE-LR/LW
WST-SFP+LR-G	SFP+	10.31 Gbps	1310nm DFB	-8.2~ 0.5dBm	PIN	-12.6dBm	-5~85°C	10km	DDM RoHS	10GBASE-LR/LW
WST-SFP+LR-I	SFP+	10.31 Gbps	1310nm DFB	-8.2~ 0.5dBm	PIN	-12.6dBm	-40~85⁰C	10km	DDM RoHS	10GBASE-LR/LW

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	04-Sep-2009	New Issue	Tina Tang	Wayne Liao	Wayne Liao
V1.1	22-Jan-2010	Add the figure for Application in System	Tina Tang	Wayne Liao	Wayne Liao
V1.2	11-Feb-2010	Add Industrial Temperature Type	Tina Tang	Wayne Liao	Wayne Liao
V2.0	14-Feb-2011	Add Extended Temperature, Modify Electrical Voltages and Company Address.	Min Liu	Wayne Liao	Wayne Liao
V2.1	14-Nov-2011	Modify photo and layout	Min Liu	Wayne Liao	Wayne Liao
VE.0	20-Oct-2020	Update Specifications & Change version	Elma Yueh	Wayne Liao	Wayne Liao
VE.1	31-May-2021	Update Drawing	ShaoYu Lee	Wayne Liao	Wayne Liao
VE.2	14-Feb-2023	Update Layout and address	ShaoYu Lee	Wayne Liao	Wayne Liao



Headquarters

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