WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G OSFP-RHS VR4 Optical Transceiver Module
P/N: WST-OR4-VR4-C

Features:

- Support 4x106G PAM4 electrical interface
- Support 4x53G PAM4 electrical interface
- Support 4x25G NRZ electrical interface
- Power consumption: 8W Max
- OSFP RHS form factor
- MMF MPO-12/APC optical connector
- Hot Pluggable module
- 3.3V power supply
- 50m max reach with MMF OM4
- Operating Case Temperature: 0℃~70℃

Applications:

- IB and Ethernet applications
- 400G SR4 multimode application
- 800G Fanout application

Standard:

- CMIS Rev. 4.0 Management Interface
- Compliant to OSFP MSA Rev. 5.0
- OSFP-RHS mechanical spec
- IEEE 802.3db: Physical Layer Specifications and Management Parameters
- RoHS10 Compliance

Absolute Maximum Ratings

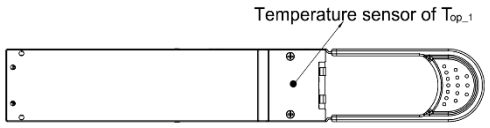
Exceeding the limits below may damage the module permanently.

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Storage Temperature	T_S	-40		85	℃	
Case Operating Temperature	T_{op_1}	0		70	℃	1, 2
Supply Voltage	VCC	-0.5		3.6	V	
Relative Humidity	RH	5		70	%	
Damage threshold, each lane		5			dBm	

Notes:

1. DDMI temperature reading is measured by the position of Top_1
2. Case operating temperature definition:

TOP view of module:



General Product Characteristics

Parameter	Value	Unit	Comments
Module Form Factor	OSFP	As defined by OSFP Rev 5.0	RHS form factor with MPO optical interface
Number of Optical Lanes	4 TX and 4 RX		
Maximum Aggregate Data Rate	103.125212.5212.5 212.5 425	Gb/s	25.78125G NRZ mode 26.5625Gbd PAM4 mode 53.125Gbd PAM4 mode
Protocols Supported	InfiniBand Ethernet		
Electrical Interface and Pin-out	60-pin edge connector		Pin-out as defined by OSFP Rev 5.0
Maximum Power Consumption	8	W	4 lanes operation, mission mode
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by CMIS Rev. 4.0

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Case Temperature	TOP	0		70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Maximum Power Consumption	P_{Con}			8	Watts	
Bit Rate	BR		53.125		GBd	
Number of Lanes	-	4				
Pre-FEC Bit Error Ratio	BER			$2.4x10^{-4}$		1
Transmit Distance	T_D			OM4 50 OM3 30	m	
Management Interface		Serial, I2C-based, maximum frequency 400 kHz				2
Logic Input Voltage High	V_{ih}	2		Vcc+3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Notes:

1. PRBS31Q test pattern is used
2. As defined by CMIS Rev. 4.0

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transmitter electrical input characteristics at TP1					
Signaling rate, each lane (nominal)		53.125+/- 100ppm		Gbd	1
Differential pk-pk voltage tolerance (min)	750			mV	
AC common-mode RMS voltage tolerance (min)	25			mV	
Differential-mode to common-mode return loss, RLcd (min)	Equation (120G-2)			mV	
Common-mode to differential-mode return loss RLdc (min)	Equation (120G-1)			dB	
Effective return loss, ERL (min)	8.5			dB	
Differential termination mismatch			10	%	
Single-ended voltage tolerance range(min)	-0.4		3.3	V	
DC common-mode voltage tolerance (range) Upper limit Lower limit	-0.35		2.85	V	
Receiver electrical output characteristics at TP4					
Signaling rate, each lane (nominal)		53.125	Gbd		
Peak-to-peak AC common-mode voltage(max) Low-frequency, $V_{CMPP-LF}$ High-frequency, $V_{CMPP-HF}$			 60 80	mV	1
Differential peak-to-peak output voltage Short mode Long mode		 600 845		mV	
Eye height (min)	15			mV	
Vertical eye closure, VEC (max)			12	dB	
Common-mode to differential-mode return loss RLdc (min)	Equation (120G-1)			dB	
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	
Transition time (min)	8.5			Ps	
DC common-mode voltage tolerance (range) Upper limit Lower limit	-0.35		2.85	V	

Note:

1. TP4 and TP1 specification are followed IEEE Draft P802.3CK/D3.2, 4th May 2022

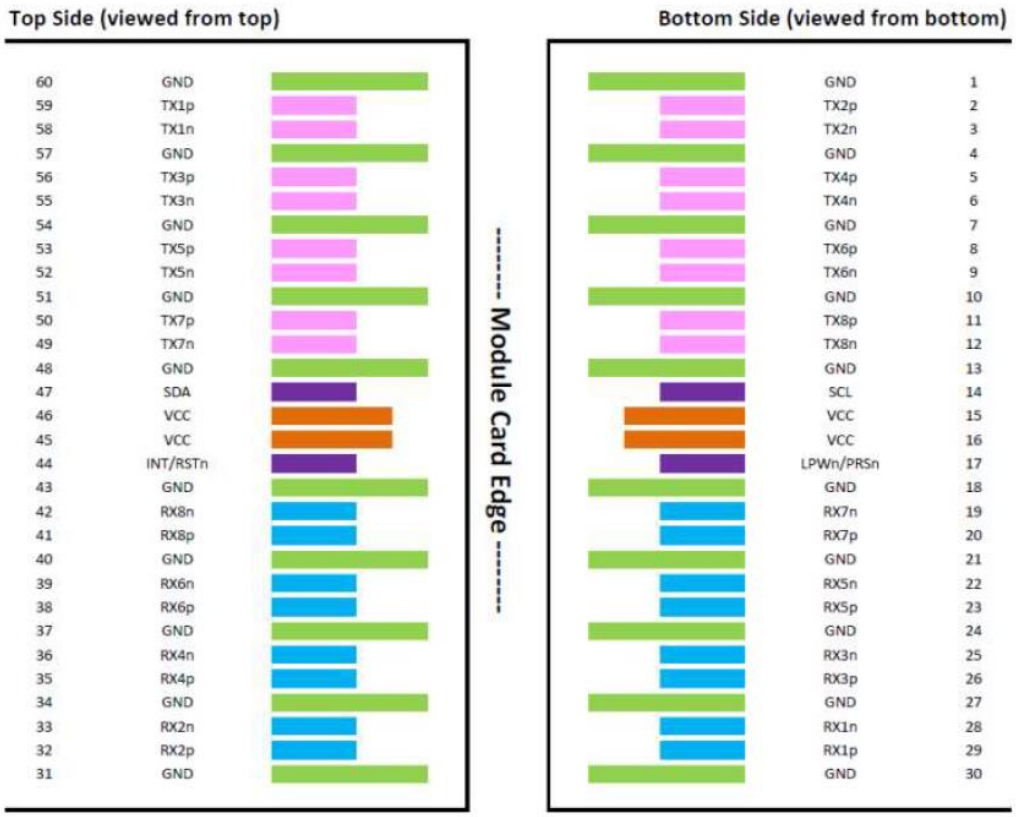
Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter						
Signaling rate, each lane (range)		53.125 ±100 ppm			GBd	
Modulation format	-	PAM4			-	
Lane Wavelength	λ	840		870	nm	
RMS spectral width				0.65	nm	
Average Optical Power	P_{avg}	-4.6		4	dBm	1
Outer Optical Modulation Amplitude (OMAouter) For TDECQ<=1.8dB For 1.8<TDECQ<-4.4dB	OMA_{outer}	 -2.6 -4.4+TDECQ		 3.5 3.5	dBm	2
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			4.4	dB	
Extinction ratio, each lane	ER	2.5			dB	
Transmitter excursion				2.3		
Average launch power at Tx off state				-30	dBm	
Relative intensity noise14 (OMA)				-132	dB/Hz	
Optical return loss tolerance				14	dB	
Receiver						
Damage threshold, each lane		5			dBm	
Average receive power, each lane		-6.3		4	dBm	
Received power (OMA), each lane				3.5	dBm	
Receiver Reflectance				-15	dB	
Receiver sensitivity (OMAouter) For TECQ<=1.8dB For 1,8<TECQ<-4.4dB				 -4.6 -6.2+TECQ		

Module Electrical Connector

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram below. It provides 16 contacts of 8 differential pairs of high-speed transmit signals, 16 contacts of 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.



PIN Descriptions (compliant with OSFP MSA Rev 5.0)

Name	Direction	Description
TX[8:1]p	Input	Transmit differential pairs from host to module
TX[8:1]n	Input	

RX[8:1]p	Output	Receiver differential pairs from module to host.
RX[8:1]n	Output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 10.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 10.5.2
VCC	Power	3.3V power for module
GND	ground	Module Ground. Logic and power return path.

PIN List

PIN	Symbol	Description	Direction	
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	Input from Host	
3	TX2n	Transmitter Data Inverted	Input from Host	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	Input from Host	
6	TX4n	Transmitter Data Inverted	Input from Host	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	Input from Host	
9	TX6n	Transmitter Data Inverted	Input from Host	
10	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	Input from Host	
12	TX8n	Transmitter Data Inverted	Input from Host	

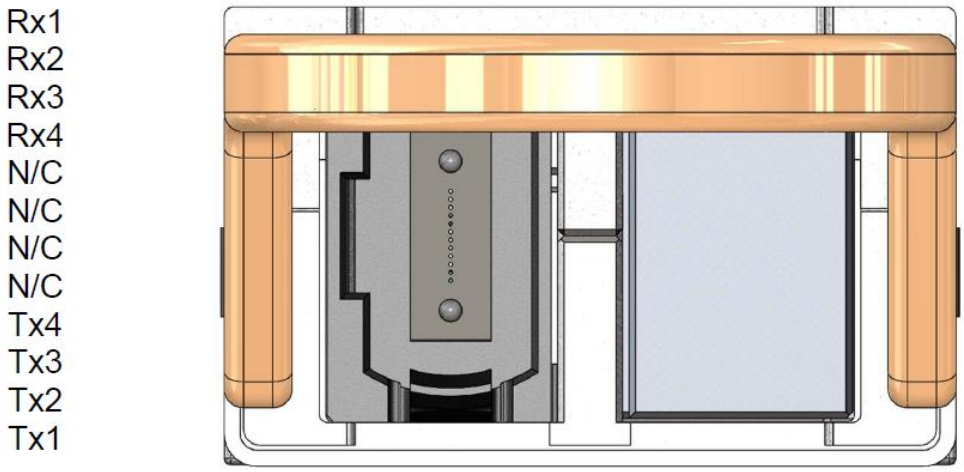
13	GND	Ground		
14	SCL	2-wire Serial interface clock	Bi-directional	Open-Drain with pull-up resistor on host
15	VCC	+3.3V Power supply	Power from Host	
16	VCC	+3.3V Power supply	Power from Host	
17	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	Open-Drain with pull-up resistor on host
18	GND	Ground		
19	RX7n	Receiver Data Inverted	Output to Host	
20	RX7p	Receiver Data Non-Inverted	Output to Host	
21	GND	Ground		
22	RX5n	Receiver Data Inverted	Output to Host	
23	RX5p	Receiver Data Non-Inverted	Output to Host	
24	GND	Ground		
25	RX3n	Receiver Data Inverted	Output to Host	
26	RX3p	Receiver Data Non-Inverted	Output to Host	
27	GND	Ground		
28	RX1n	Receiver Data Inverted	Output to Host	
29	RX1p	Receiver Data Non-Inverted	Output to Host	
30	GND	Ground		
31	GND	Ground		
32	RX2n	Receiver Data Inverted	Output to Host	
33	RX2p	Receiver Data Non-Inverted	Output to Host	
34	GND	Ground		
35	RX4n	Receiver Data Inverted	Output to Host	
36	RX4p	Receiver Data Non-Inverted	Output to Host	
37	GND	Ground		
38	RX6n	Receiver Data Inverted	Output to Host	
39	RX6p	Receiver Data Non-Inverted	Output to Host	

40	GND	Ground		
41	RX8n	Receiver Data Inverted	Output to Host	
42	RX8p	Receiver Data Non-Inverted	Output to Host	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	See pin description for required circuit
45	VCC	+3.3V Power supply	Power from Host	
46	VCC	+3.3V Power supply	Power from Host	
47	SDA	2-wire Serial interface data	Bi-directional	Open-Drain with pull-up resistor on HOST
48	GND	Ground		
49	TX7p	Transmitter Data Non-Inverted	Input from Host	
50	TX7n	Transmitter Data Inverted	Input from Host	
51	GND	Ground		
52	TX5p	Transmitter Data Non-Inverted	Input from Host	
53	TX5n	Transmitter Data Inverted	Input from Host	
54	GND	Ground		
55	TX3p	Transmitter Data Non-Inverted	Input from Host	
56	TX3n	Transmitter Data Inverted	Input from Host	
57	GND	Ground		
58	TX1p	Transmitter Data Non-Inverted	Input from Host	
59	TX1n	Transmitter Data Inverted	Input from Host	
60	GND	Ground		

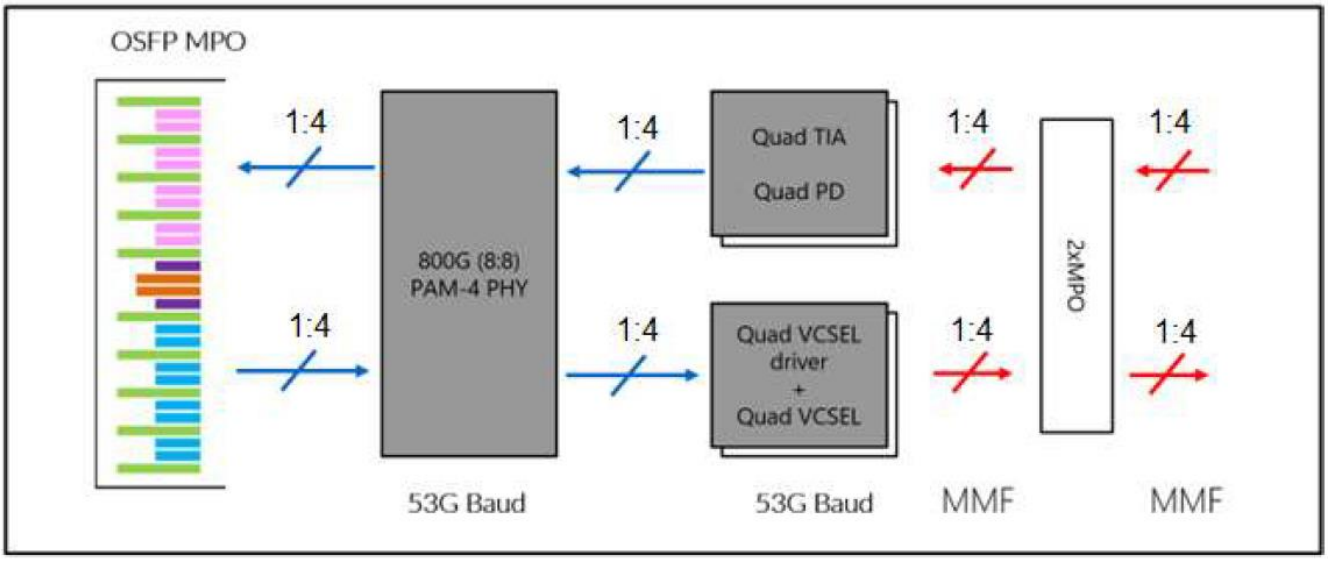
Transceiver Optical MPO Connectors

Below picture shows channel orientation of the optical connector when MPO-12 connectors are used in an OSFP module.

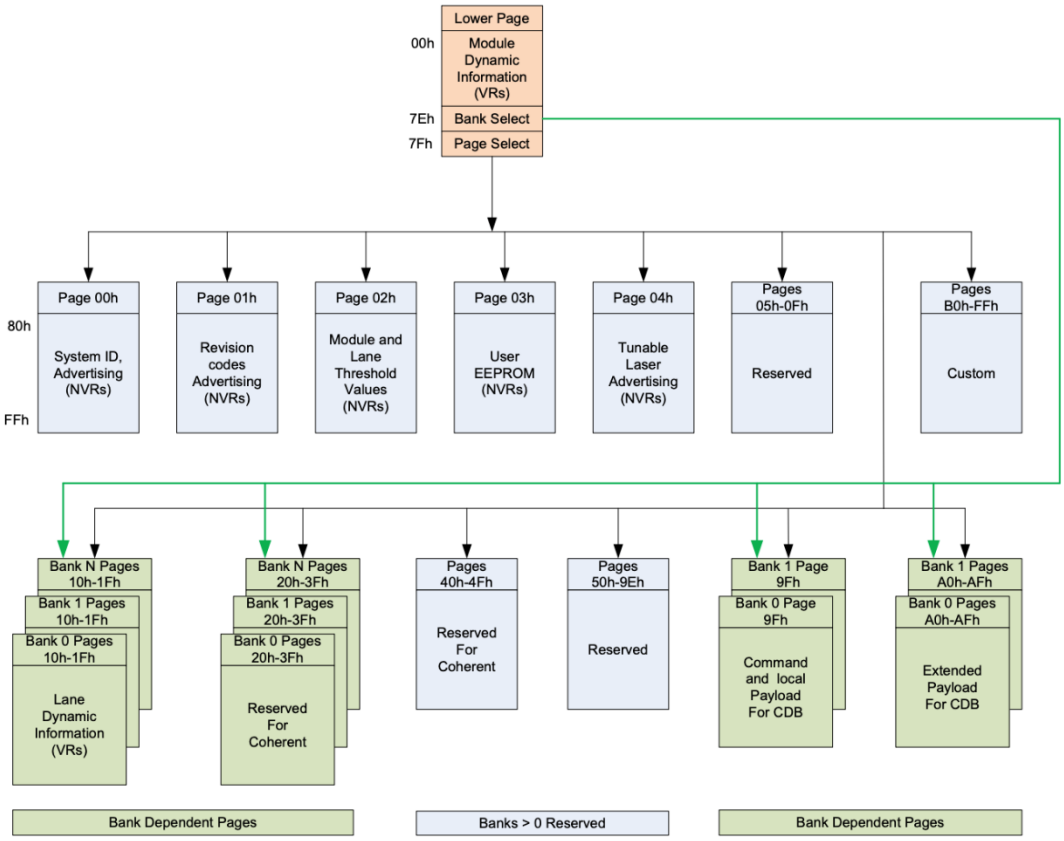
MPO-12 connectors, which channel assignment within the connector to be as in the below picture.

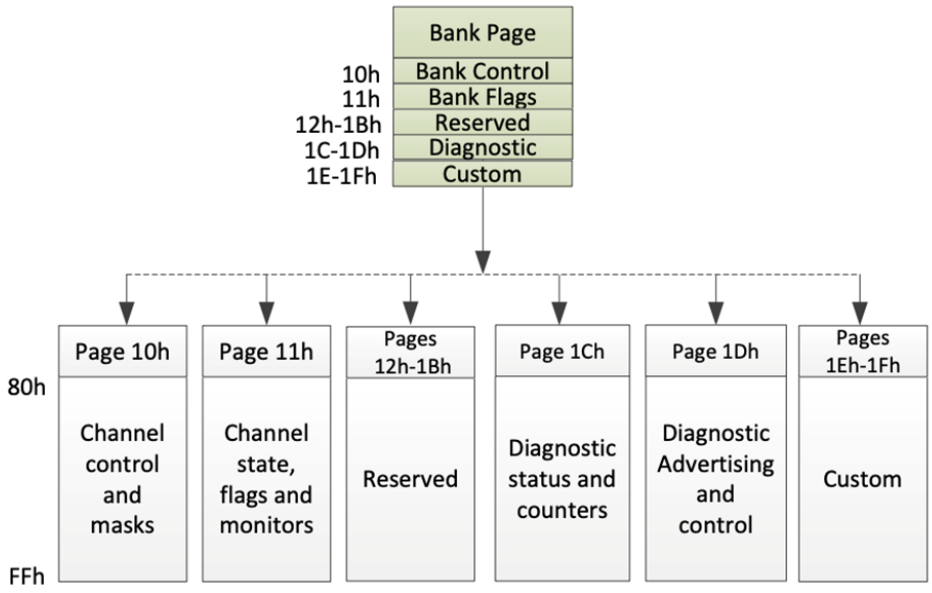


Transceiver Block Diagram

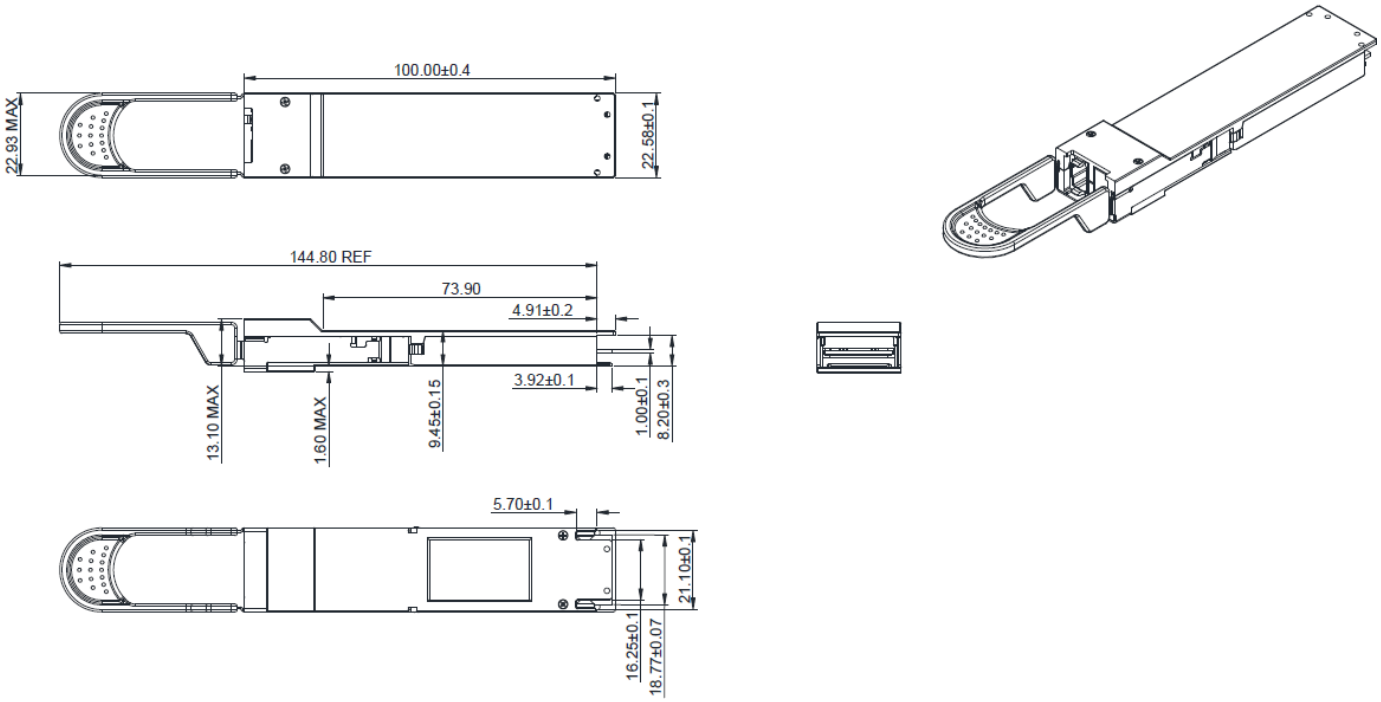


Memory Map ((compliant with CMIS Rev. 4.0))





Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power (OMAouter)	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-OR4-VR4-C	OSFP RHS	53.125Gbd (PAM4) each Channel	850nm EML	-2.6 ~ +3.5 -4.4+TDECQ ~ +3.5 dBm each Channel	PIN	-4.6 -6.2+TECQ dBm each Channel	0~70°C	OM4 50m OM3 30m	DDM RoHS	400G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	09-Jul-2024	New Release	Joanne Ni	Ken Cheng	Wayne Liao
V1.1	19-Jul-2024	Added optical fiber type as MPO-12/APC	Joanne Ni	Ken Cheng	Wayne Liao

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