WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

800G OSFP-RHS 2xDR4 500m Transceiver

P/N: WST-OR8-DR4X2-C

Features:

- 800G 2xDR4 single mode transceiver
- 8-channels of 100G-PAM4 electrical modulation
- Two ports of 4-channel 100G-PAM4 optical modulation
- Two MPO12/APC optical connectors
- OSFP RHS form factor
- Silicon photonics integration solution based on 1310nm CW laser light source
- 16W max power consumption
- 500m max reach with SMF
- 3.3V power supply
- Operating Case Temperature: 0 to 70°C

Applications:

- Ethernet for 8x100G, 4x200G, 2x400G
- IB for 2xNDR, 4xNDR200

Standards:

- Compliant to OSFP MSA Rev. 5.0
- Compliant to IEEE Std 802.3bs-2017 for Optical Interface
- Compliant to IEEE Std 802.3ck-2022 for Electrical Interface
- CMIS Rev. 4.0 Management Interface
- Compliant to Class 1 Laser Safety
- ROHS-6: Environment Safety

General Product Characteristics

Parameter	Value	Unit	Comments
Module Form Factor	OSFP RHS	-	As defined by OSFP MSA Rev. 5.0
Number of Optical Lanes	8 TX and 8 RX	-	
Maximum Aggregate Data Rate	850	Gb/s	
Protocols Supported	Ethernet	-	
Electrical Interface and Pin-out	60-pin edge connector	-	As defined by OSFP MSA Rev. 5.0
Optical Interface	Type 1 MPO16/APC	-	As defined by OSFP MSA Rev. 5.0
Maximum Power Consumption	16	W	
Management Interface	Serial, I2C-based, 400 kHz maximum frequency	-	As defined by CMIS Rev. 4.0

Absolute Maximum Ratings

Absolute maximum ratings are those beyond which damage to the device may occur. Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	°C	
Operating Relative Humidity	RH	5	95	%	Note1
Power Supply Voltage	VCC	-0.5	3.6	V	
Data Input Voltage Differential	IVDIP-VDINI		1	V	
Control Input Voltage	VIN	-0.3	VCC+0.5	V	
Control Output Current	Io	-20	20	mA	

Note:

1. Non-condensing

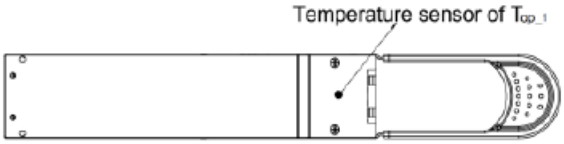
Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Operating Case Temperature	T_{OP_1}	0		60	°C	1, 2
	T_{OP_2}	0		70	°C	2
Module Power Dissipation	P			16	W	Tcase =70℃
Signaling Speed per Lan	BR		53.125		GBd	
Number of Lanes		8				
Pre-FEC Bit Error Ratio				2.4x10-4	-	3
Transmit Distance	T_D			500	m	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)				25	mV	
Rx Differential Data Output Load			100		Ohm	

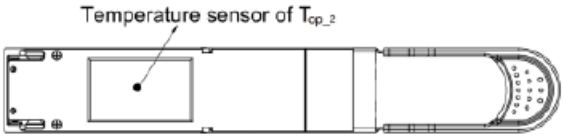
Note:

1. DDMI temperature reading is measured by the position of Top_1
2. Case operating temperature definition:

TOP view of module:



Bottom view of module:



3. PRBS13Q test pattern is used & FEC is provided by host system.

Electrical Characteristics (Compliant with IEEE 802.3ck-2022 400GAUI-4 C2M)

Parameter	Min	Typical	Max	Units	Notes
Receiver at TP4 (Module output, 802.3ck Table 120G–3)					
Peak-to-peak AC common-mode voltage			32 80	mV	
Differential peak-to-peak output voltage			600 845	mV	
Eye height	15			mV	
Vertical eye closure			12	dB	
Effective return loss	8.5				
Differential to Common Mode Input Return Loss	IEEE 802.3-ck Equation (120G-2)			dB	
Differential termination mismatch			10	%	
Transition time	8.5			ps	
DC common-mode voltage tolerance	-350		2850	mV	
Transmitter at TP1&TP1a (Module input, 802.3ck Table 120G–9)					
Differential pk-pk voltage tolerance	750			mV	
Peak-to-peak AC common-mode voltage tolerance	32 80			mV	
Common-mode to differential-mode return loss	802.3ck Equation (120G–1)			dB	
Effective return loss	8.5			dB	
Differential termination mismatch			10	%	

Module stressed input tolerance	See 802.3ck 120G.3.4.3				
Single-ended voltage tolerance range	-0.4		3.3	V	
DC common-mode voltage tolerance	-0.35		2.85	V	

Electric Specification for Low Speed Signal

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Module output SCL&SDA	V_{OL}	0	-	0.4	V	
	V_{OH}	VCC-0.5	-	VCC+0.3	V	
Module input SCL&SDA	V_{IL}	-0.3	-	VCC*0.3	V	
	V_{IH}	VCC*0.7	-	VCC+0.5	V	
IntL/RxLos	V_{OL}	0	-	0.4	V	
	V_{OH}	VCC-0.5	-	VCC+0.3	V	
LPMode/TxDis, ResetL, ModSeIL	V_{IL}	-0.3	-	0.8	V	
	V_{IH}	2	-	VCC+0.3	V	

Optical Characteristics (Compliant with IEEE 802.3bs-2017 400GBASE-DR4)

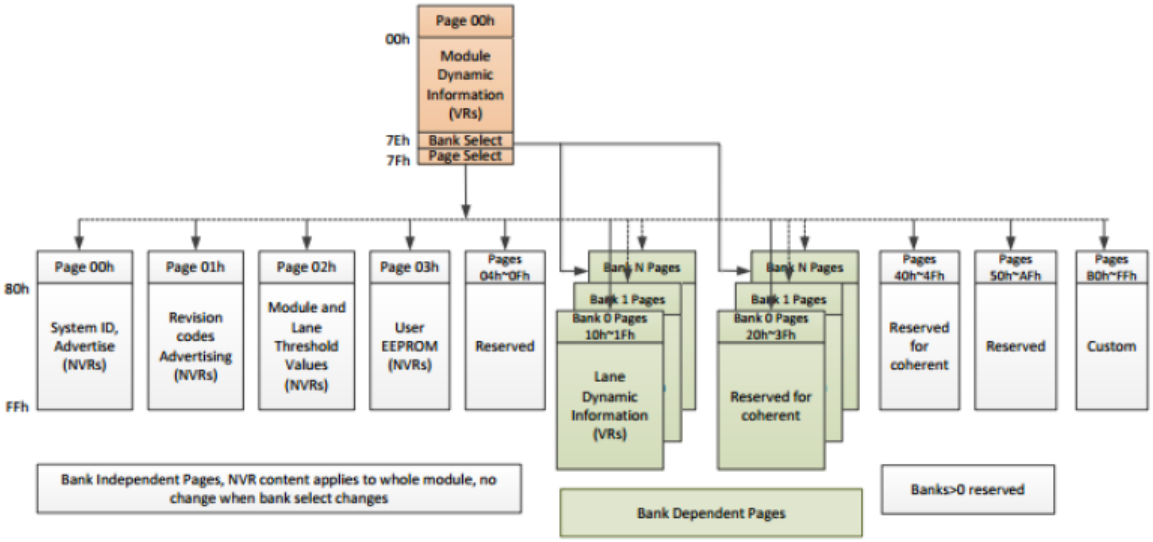
Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter (Module output, 802.3bs Table 124–6)						
Optical Data Rate per channel（PAM4）	DR	53.125±100ppm			GBd	
Modulation Format		PAM4				
Wavelength Assignment	λ	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Optical Power	Pavg	-2.9		4	dBm	1
Outer Optical Modulation Amplitude	OMAouter	-0.8		4.2	dBm	2
Launch power in OMA minus TDECQ, each lane		-2.2			dBm	
Transmitter and Dispersion Eye Closure Penalty	TDECQ			3.4	dB	
Average Launch Power of OFF Transmitter, each Lane				-15	dB/Hz	
Extinction Ratio	ER	3.5			dB	

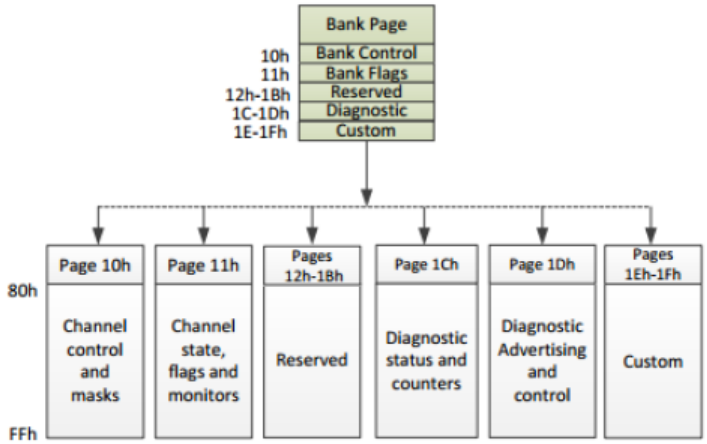
$RIN_{21.4}OMA$				-136	dB/Hz	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	3
Receiver(Module input, 802.3bs Table 124–7)						
Optical Data Rate per channel（PAM4）	DR	53.125±100ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each lane		5			dBm	4
Line wavelengths	λ	1304.5	1311	1317.5	nm	
Average receiver power, each lane		-5.9		4	dBm	5
Receiver power, each lane (OMA)				4.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lanec (max)				-4.4	dBm	6
Stressed receiver sensitivity (OMAouter), each laned (max)				-1.9	dBm	7
Conditions of stressed receiver sensitivity test:						8
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	
OMAouter of each aggressor lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.
3. Transmitter reflectance is defined looking into the transmitter
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
7. Measured with conformance test signal at TP3 (see 124.8.9) for the BER specified 124.1.1.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

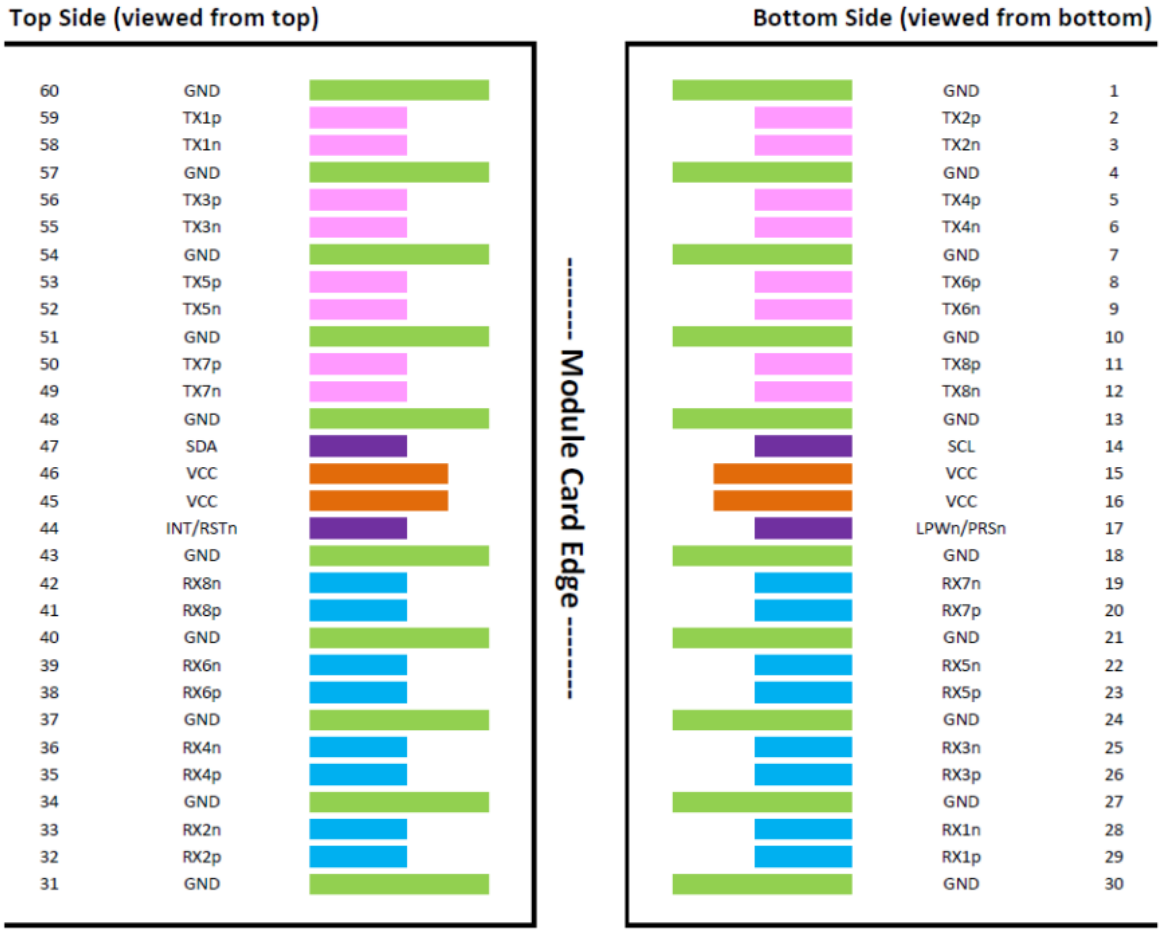
MEMORY MAP (compliant QSFP-DD Rev. 4.0)





Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Pin Assignment



Module Signal PIN Descriptions (compliant OSFP MSA Rev 5.0)

Name	Direction	Description
TX[8:1]p	input	Transmit differential pairs from host to module.
TX[8:1]n	input	
RX[8:1]p	output	Receiver differential pairs from module to host.
RX[8:1]n	output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 10.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host

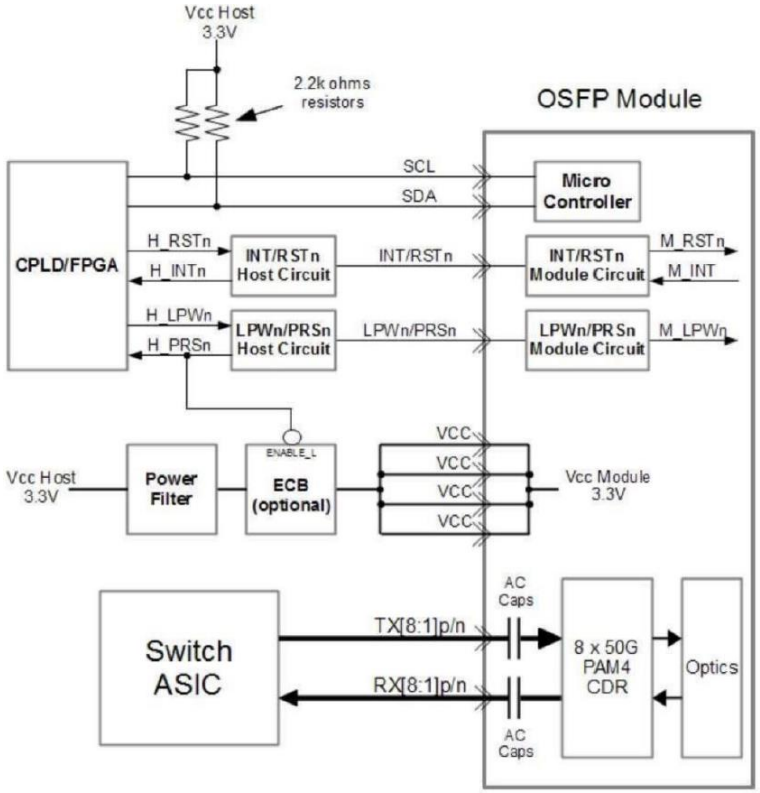
		to module. This signal requires the circuit as described in Section 10.5.2
VCC	power	3.3V power for module.
GND	ground	Module Ground. Logic and power return path.

Module Signal PIN Lists (compliant OSFP MSA Rev 5.0)

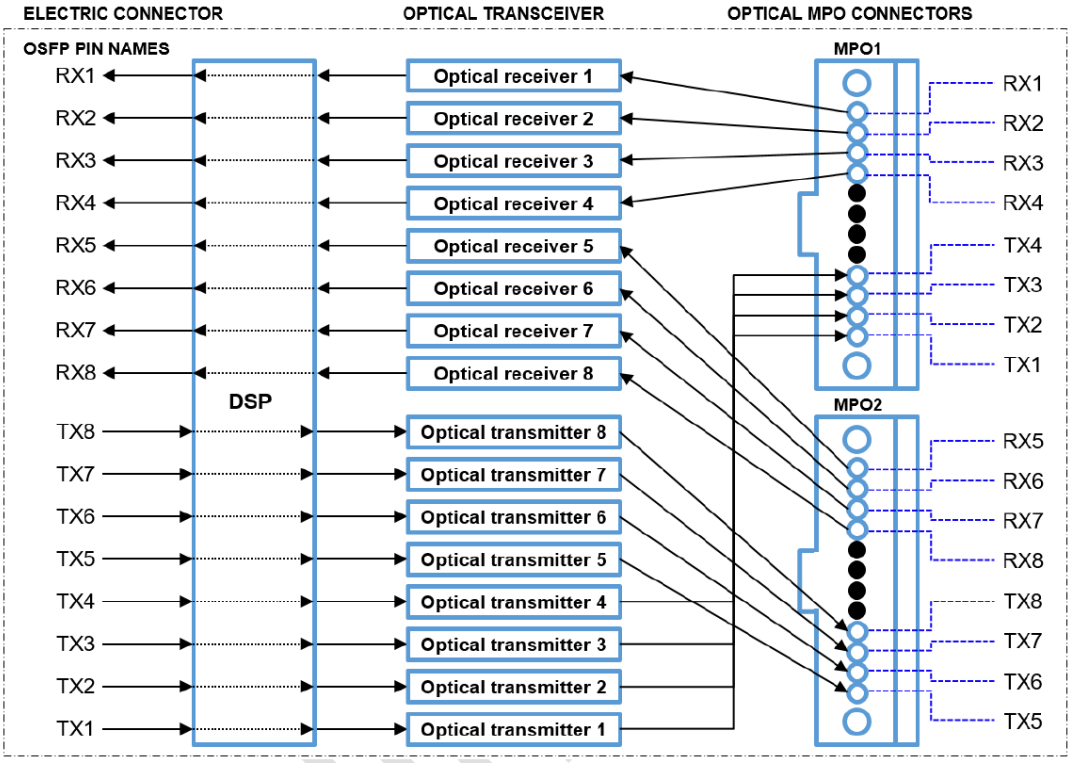
Pin	Symbol	Description	Plug Sequence
1	GND	Ground	1
2	TX2p	Transmitter Data Non-Inverted	3
3	TX2n	Transmitter Data Inverted	3
4	GND	Ground	1
5	TX4p	Transmitter Data Non-Inverted	3
6	TX4n	Transmitter Data Inverted	3
7	GND	Ground	1
8	TX6p	Transmitter Data Non-Inverted	3
9	TX6n	Transmitter Data Inverted	3
10	GND	Ground	1
11	TX8p	Transmitter Data Non-Inverted	3
12	TX8n	Transmitter Data Inverted	3
13	GND	Ground	1
14	SCL	2-wire Serial interface clock	3
15	VCC	+3.3V Power	2
16	VCC	+3.3V Power	2
17	LPWn/PRSn	Low-Power Mode / Module Present	3
18	GND	Ground	1
19	RX7n	Receiver Data Inverted	3
20	RX7n	Receiver Data Non-Inverted	3
21	GND	Ground	1
22	RX5n	Receiver Data Inverted	3
23	RX5p	Receiver Data Non-Inverted	3
24	GND	Ground	1
25	RX3n	Receiver Data Inverted	3
26	RX3p	Receiver Data Non-Inverted	3
27	GND	Ground	1
28	RX1n	Receiver Data Inverted	3
29	RX1p	Receiver Data Non-Inverted	3

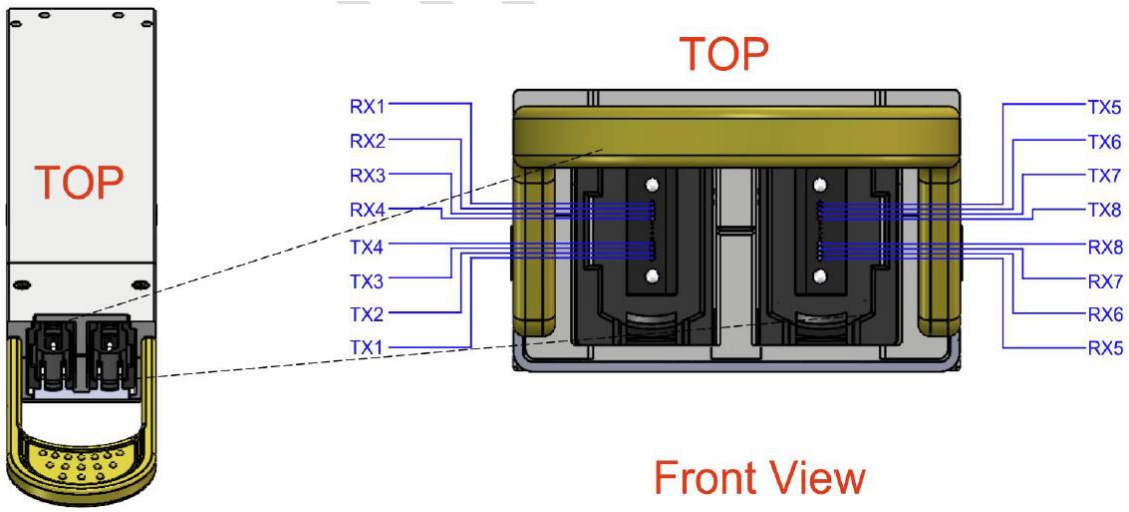
30	GND	Ground	1
31	GND	Ground	1
32	RX2p	Receiver Data Non-Inverted	3
33	RX2n	Receiver Data Inverted	3
34	GND	Ground	1
35	RX4p	Receiver Data Non-Inverted	3
36	RX4n	Receiver Data Inverted	3
37	GND	Ground	1
38	RX6p	Receiver Data Non-Inverted	3
39	RX6n	Receiver Data Inverted	3
40	GND	Ground	1
41	RX8p	Receiver Data Non-Inverted	3
42	RX8n	Receiver Data Inverted	3
43	GND	Ground	1
44	INT/RSTn	Module Interrupt / Module Reset	3
45	VCC	+3.3V Power	2
46	VCC	+3.3V Power	2
47	SDA	2-wire Serial interface data	3
48	GND	Ground	1
49	TX7n	Transmitter Data Inverted	3
50	TX7p	Transmitter Data Non-Inverted	3
51	GND	Ground	1
52	TX5n	Transmitter Data Inverted	3
53	TX5p	Transmitter Data Non-Inverted	3
54	GND	Ground	1
55	TX3n	Transmitter Data Inverted	3
56	TX3p	Transmitter Data Non-Inverted	3
57	GND	Ground	1
58	TX1n	Transmitter Data Inverted	3
59	TX1p	Transmitter Data Non-Inverted	3
60	GND	Ground	1

Recommended Circuit

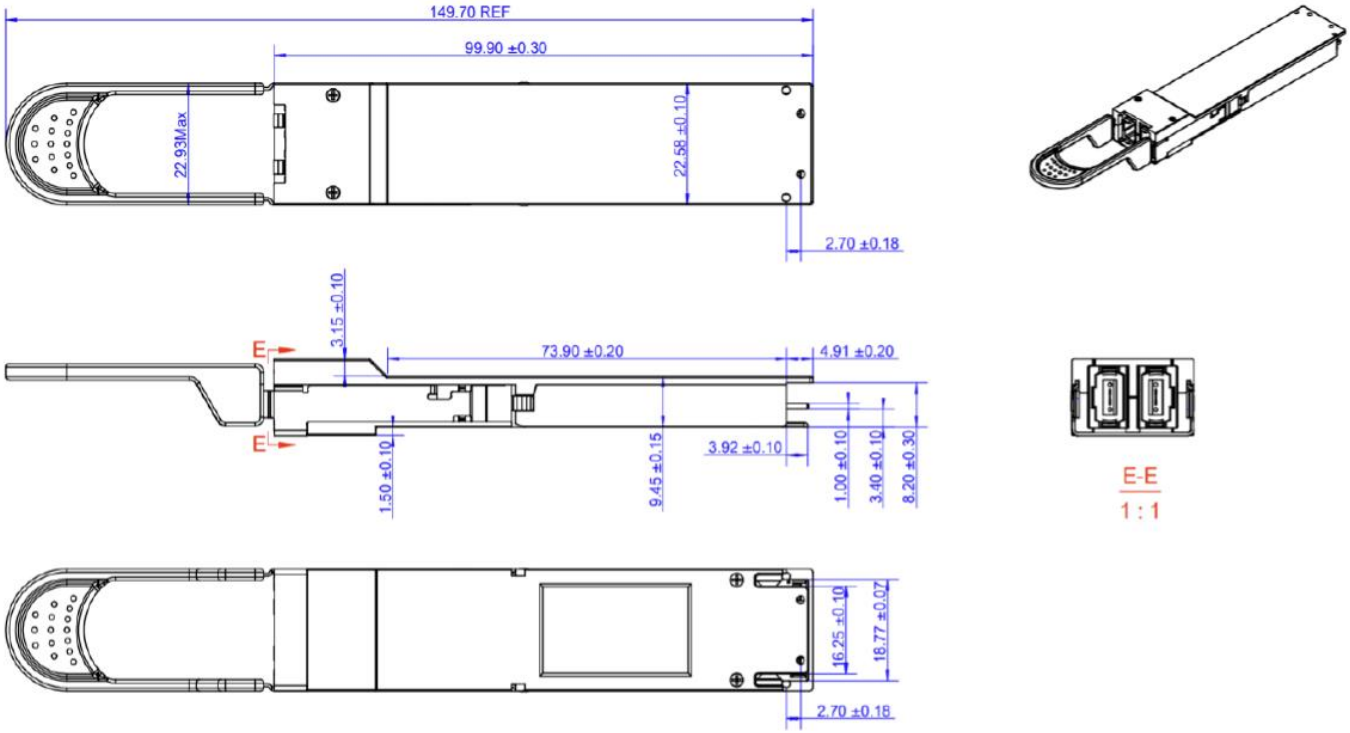


Block Diagram of Transceiver





Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-OR8-DR4X2-C	OSFP-RHS	53.125Gbps (PAM4) per channel	1310 nm	-2.9~ +4 dBm	PIN	> -4.4	0~70°C	500m	DDM RoHS	800G 2xDR4

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	30-Aug-2024	New Issue	Joanne Ni	Ken Cheng	Wayne Liao

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