Data Sheet

4x100G-LR1 QSFP-DD 10km Transceiver Module
P/N: WST-QD4-PLR4-C

Applications:

- Data Center Interconnect
- Data Center 400GE 10 km SMF links
- 400GE to 4x 100GE breakout over 10 km
- 400GE Metro Ethernet

Standard:

- QSFP-DD MSA compliant
- CMIS 4.0 management interface

Features:

- Breakout Mode
  - 4x 100GBASE-LR1 compliant 53.125GBd PAM4
  - 4x 100GAUI-2 compliant 2x 26.5625 GBd PAM4
- Aggregation Mode
  - 400 Gb/s Ethernet Protocol 4x 53.125GBd PAM4
  - 400GAUI-8 compliant 8x 26.5625 GBd PAM4
- MPO-12 connector with 8° angled end-face
- Power consumption <12 W
- Operating case temperature 0 to 70 ºC

Description

Wavesplitter's WST-QD4-PLR4-C is a fully integrated, 425 Gb/s optical transceiver for links up to 10 km by means PSM to the transmit and receive ports of the MPO-12 connector. In Breakout Mode, WST-QD4-PLR4-C is complied with the optical interface specification IEEE Std 802.3-2018 Section 8 100GBASE-LR1 per lane. 100GBASE-LR1 specifies the use of PAM4 at 53.125 Gbaud operating at the channel with wavelength on the range of 1304.5-1317.5 nm from cooled EA-DFB-LDs and WST-QD4-PLR4-C has four of the lanes with 100GBASE-LR1. The bit rate per lane is 106.25 Gb/s. The received optical lanes are specified by 100GBASE-LR1 per lane and paralleled from the receive MPO-12 connector ports to 4 PIN-PDs with transimpedance amplifiers (TIAs) to recover the PAM4 for interfacing with the electrical interface.

The electrical interface is in compliance with 100GAUI-2 specified in IEEE Std 802.3-2018 Section 6. 100GAUI-2 specifies the use of two differential electrical lanes operating at 26.5625 GBd PAM4 per lane. The bit rate per lane is 53.125 Gb/s. WST-QD4-PLR4-C has four sets of the two lanes specified by 100GAUI-2. By means of a 2:1 mux/demux in DSP, 100GBASE-LR1 optical interface is connected to 100GAUI-2 electrical interface.

In addition, by selecting Aggregation Mode, WST-QD4-PLR4-C transmits aggregated data rate of 425Gbps. The aggregated data specifies the use of PAM4 at 53.125 Gbaud operating at four parallel channels. The bit rate per lane is 106.25

Gb/s, which produces an aggregate data rate of 425 Gb/s by means PSM to the transmit ports of the MPO-12 connector. The received optical lanes are paralleled from the receive MPO- 12 connector ports to recover the PAM4 for interfacing with the electrical interface. 400GAUI-8 specifies the use of eight differential electrical lanes operating at 26.5625 GBd PAM4 per lane. The bit rate per lane is 53.125 Gb/s, resulting in an aggregate data rate of 425 Gb/s that matches the optical line interface. An internal gear box IC converts between the eight lanes of the host interface and the four lanes of the line interface.

The bit error ratio (BER) of the optical interface is required by 100GBASE-R (Breakout Mode) and 400GBASE-R (Aggregation Mode) to be less than 2.4×10^{-4}. The host side shall have Forward Error Correction (FEC) capability based on RS(544,514) requirements defined by IEEE Std 802.3-2018 Section 8 to meet the frame loss ratio requirements of 4x 100GE and 400GE.

The form factor of WST-QD4-PLR4-C is QSFP56-DD Type 2A and is compliant with the hardware and Common Management Interface Specifications (MIS) of the QSFP-DD multi-source agreement (MSA). QSFP-DD modules can support up to eight electrical lanes on the host interface, which is double the number of lanes supported by QSFP28 or QSFP+ modules. The unique feature of QSFP-DD ports is that they are mechanically and electrically compatible with QSFP28 and QSFP+. Hence, the same port can be used to support multiple generations of modules and data rates if the networking hardware is designed for such operation.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	°C	
Power Supply Voltage	Vcc	0	3.6	V	
Optical Receiver Input (each lane)			+5.8	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	TOP	0		70	°C	
Supply Voltage Noise Tolerance	$PSNR_{mod}$			66	mV	10 Hz –10 MHz
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Consumption	P_6			12	W	
Instantaneous peak current	Icc_ip_6			4800	mA	
Sustained peak current	Icc-sp_6			3960	mA	
Supply Current	Icc-6			3827.8	mA	Steady state

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Min	Typical	Max	Units	Notes
Module output (each lane, at TP4) (Note 1)					
Signaling Rate, each Lane	26.5625 ± 100 ppm			GBd	
AC Common-mode output voltage (RMS)			17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)	0.265			UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)	0.2			UI	
Far-end Eye height, differential	30			mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	Equation (83E-2)			dB	2
Common to differential mode conversion return loss	Equation (83E-3)			dB	2
Differential termination mismatch			10	%	
Transition time (20% to 80%)	9.5			ps	
DC common mode voltage	-350		2850	mV	
Module input (each lane)					
Signaling Rate, each Lane	26.5625 ± 100 ppm			GBd	
Differential pk-pk input voltage tolerance	900			mV	at TP1a

Differential input return loss	Equation (83E-5)			dB	at TP1, 2
Differential to common mode input return loss	Equation (83E-6)			dB	at TP1, 2
Differential termination mismatch			10	%	at TP1
ESMW (Eye symmetry mask width)	0.22			UI	at TP1a
Eye width	0.22			UI	at TP1a
Applied pk-pk sinusoidal jitter	Table 120E–6			MHz, UI	at TP1a
Eye height	32			mV	at TP1a
Single-ended input voltage tolerance range	-0.4		3.3	V	at TP1a
DC common mode voltage	-350		2850	mV	at TP1

Notes:

1. Electrical module output is squelched for loss of optical input signal.
2. IEEE Std 802.3-2018 Section 6.

Optical Characteristics

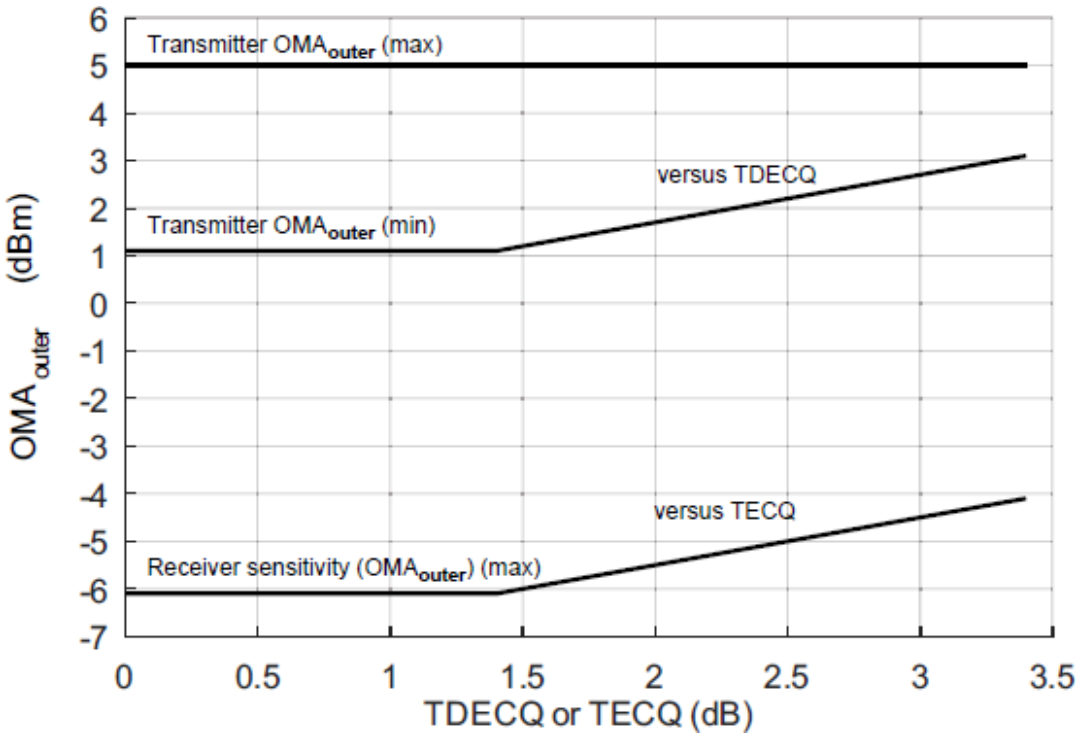
Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Wavelength Assignment	λ_C	1304.5		1317.5	nm	
Channel data rate	f_{DC}	106.25			Gbit/s	
Data Rate, each Lane	f_{SG}	53.125 ± 100 ppm			GBd	PSM4
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane		-1.9		4.8	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane [Figure 3]		1.1		5	dBm	for TDECQ <1.4 dB
		-0.3+ TDECQ				for 1.4 dB ≤ TDECQ ≤ 3.4 dB
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Transmitter eye closure for PAM4, each lane	TECQ			3.4	dB	
| TDECQ – TECQ |				2.5	dB	
Average optical output power of OFF Transmitter, each lane	Poff			-15	dBm	

Extinction Ratio, each lane	ER	3.5			dB	
Transmitter transition time				17	ps	
Transmitter over/under-shoot				22	%	
Transmitter power excursion				2.8	dBm	
$RIN_{15.6}OMA$				-136	dB/Hz	
Optical return loss tolerance				15.6	dB	
Transmitter reflectance				-26	dB	2
Receiver						
Average receive power, each lane		–8.2		4.8	dBm	3
Receive power (OMAouter) , each lane				5.0	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane [Figure 3]		Max -6.1			dBm	for TECQ <1.4 dB, 4
		Max (-7.5 + TECQ)				for 1.4 dB ≤ TECQ ≤ 3.4 dB, 4
Stressed receiver sensitivity, each lane (OMAouter)				-4.1	dBm	4, 5
Conditions of stressed receiver sensitivity test (note 6)						
Stressed eye closure for PAM4, lane under test	SECQ	3.4			dB	
LOS Assert	LOSA	-15		-9.6	dBm	
LOS De-assert	LOSD			-9.1	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. For when Pre-FEC BER is 2.4×10^{-4}.
5. Measured with conformance test signal at TP3 (see IEEE P802.3cu clause 140.7.10) for the BER specified in IEEE P802.3cu clause 140.1.1.

6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



MEMORY MAP (compliant QSFP-DD Rev. 4.0)

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Digital Diagnostic Functions

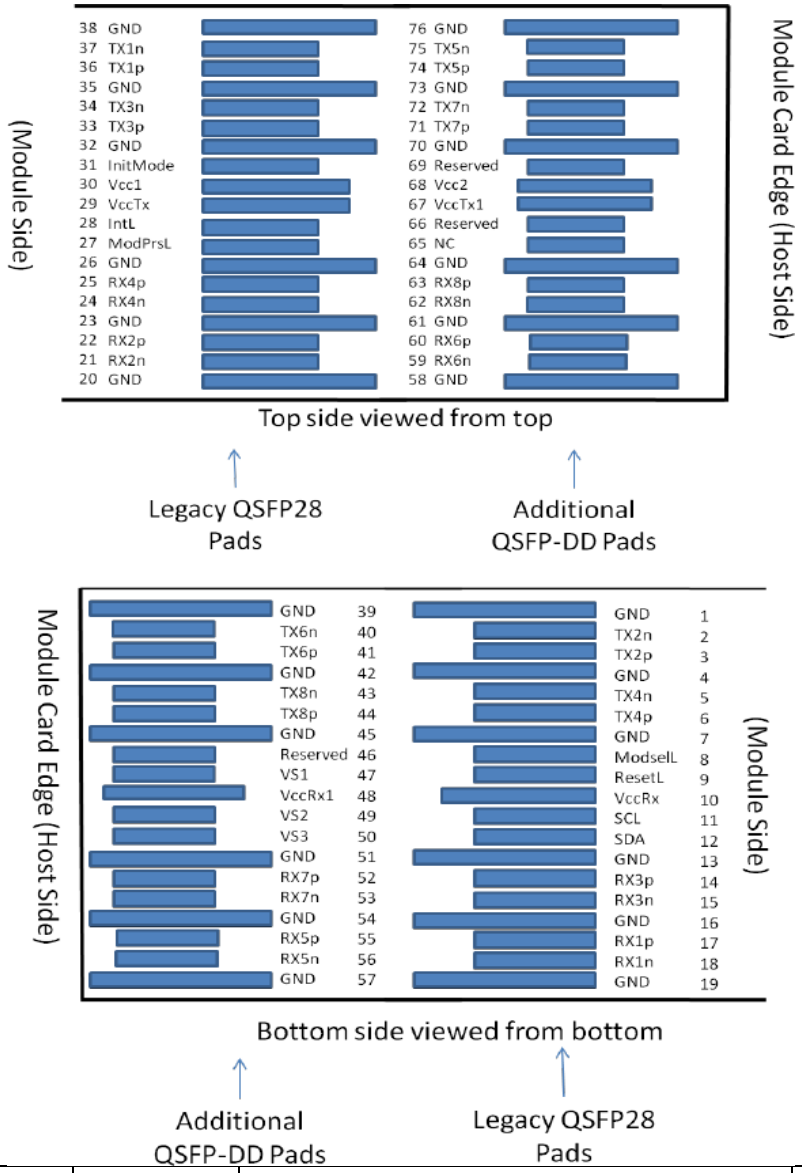
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Pin Assignment

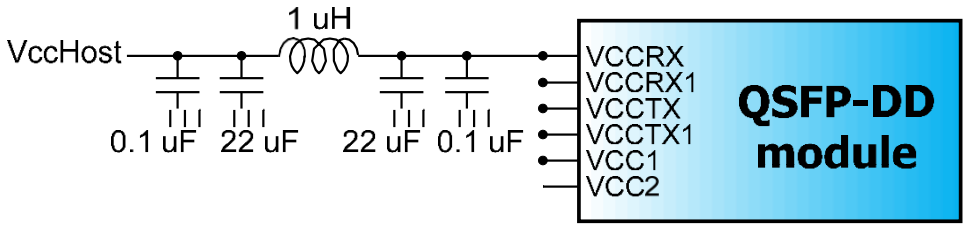


Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	

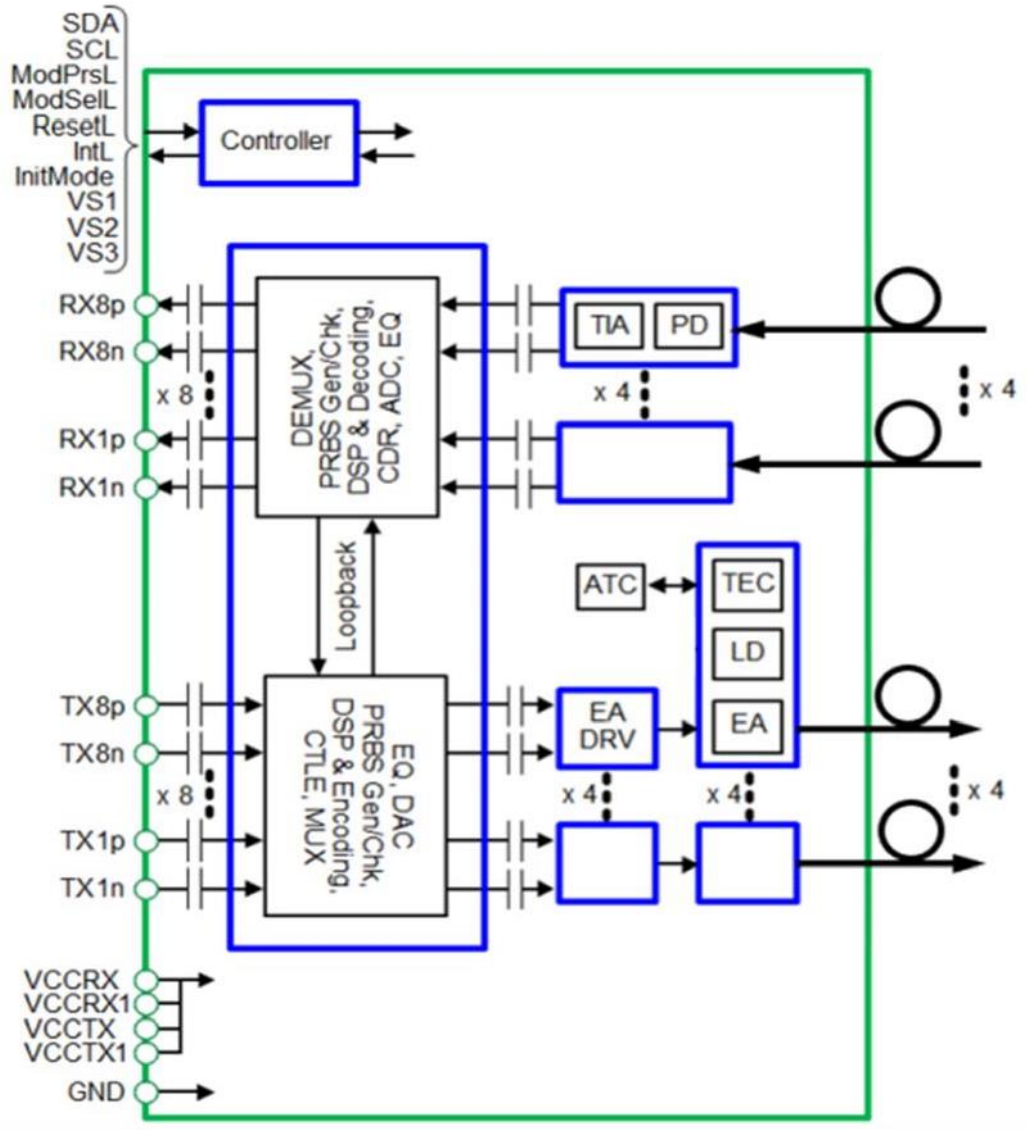
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	1
16		GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	

45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

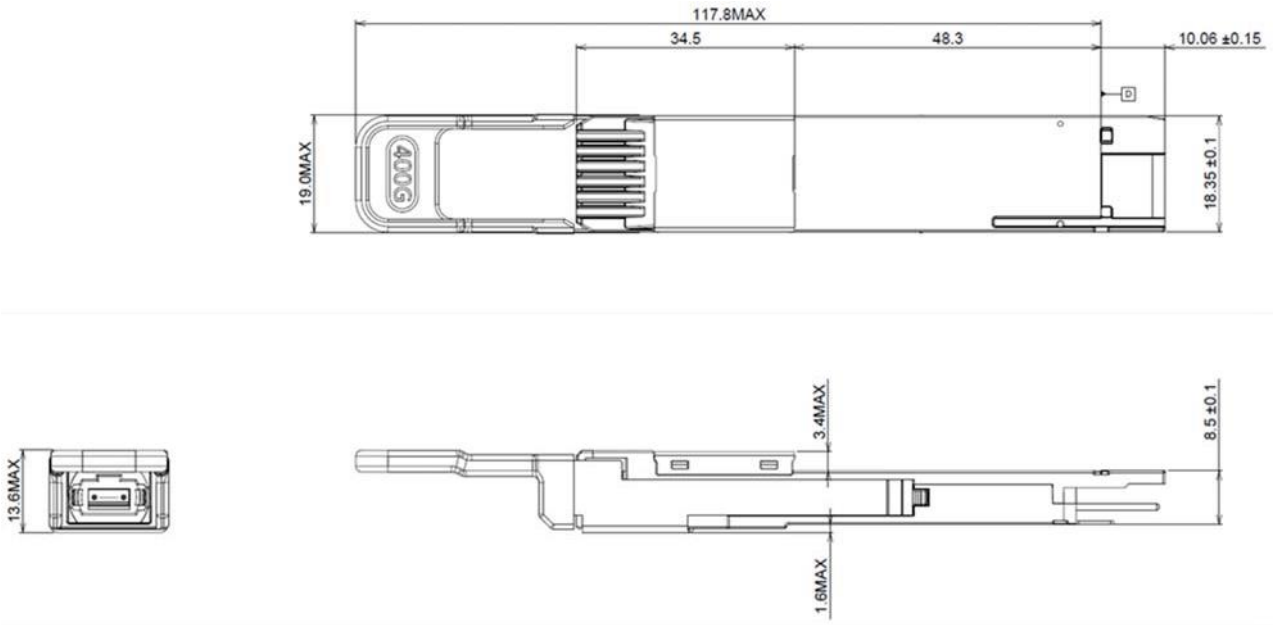
Recommended Power Supply Filter



Recommended Host - Transceiver Interface Block Diagram



Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Max. Receive Sensitivity	Temp	Reach	Other	Application code
WST-QD4-PLR4-C	QSFP-DD	106.25Gbps (PAM4) per channel	1304.5~1317.5nm EML	-1.9~ +4.8 dBm each Channel	PIN	-8.2~4.8 dBm each Channel	0~70°C	10km	DDM RoHS	400G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	08-Jun-2022	New Issue	ShaoYu Lee	Tom Tang	Wayne Liao

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