Preliminary Data Sheet

400G QSFP-DD to OSFP(RHS) Active Optical Cable (AOC

P/N: WS-D4O4-AOCxCxx4

Features:

- Hot Pluggable QSFP-DD and OSFP(RHS) Cable End
- Supports 425Gb/s aggregate bit rate
- Low Power Dissipation, Max. 8W at QSFP-DD end and Max. 9W at OSFP end
- 8x50G PAM4 VCSEL/PIN photo detector
- Operating Case Temperature: 0~70℃
- Compliant to Class 1M Laser Safety

Standard:

- Compliant to QSFP-DD Rev 6.3
- Compliant to OSFP Rev 5.0
- CMIS Rev. 4.0 Management Interface
- SFF-8679: General Electrical
- IEEE 802.3bs: Physical Layer Specifications and Management Parameters

Applications:

- Ethernet for 400GBASE-SR8
- HPC and AI Interconnects
- Proprietary Interconnection

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes.
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-40		85	℃	
Case Operating Temperature	T_{op}	0		70	℃	
Relative Humidity	RH	0		85	%	1

Notes:

1 No-condensing.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes
Supply Voltage	V_{cc}	3.14		3.46	V	
Power Consumption	P_{Con}			8	W	QSFP-DD
				9	W	OSFP-RHS
Bit Rate	BR		26.5625		GBd	1
Pre-FEC Bit Error Ratio	BER			$2.4x10^{-4}$		2
Post-FEC Bit Error Ratio				10^{-12}		
Center wavelength	λ_c	840		860	nm	3
Beam divergence angle			23		°	
Number of Lanes		8				
Management Interface		Serial, I2C-based, maximum frequency 400 kHz				4
Logic Input Voltage High	V_{ih}	2		Vcc+0.3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Notes:

1 Single lane

2 PRBS13Q test pattern is used.

3 As defined by IEEE Std. 802.3cd™ /D3.0

4 As defined by CMIS Rev. 4.0

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Notes
Transceiver Power Supply Current	I_{cc}			2400	mA	
Transmitter at TP1a						
AC common-mode output voltage(RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitter disabled)				35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)				880	mV	
Eye symmetry mask width	ESMW		0.22		UI	
Eye height, differential	EH	32			mV	

Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch				10	%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
Receiver at TP4						
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch				10	%	
Transition time (20% to 80%)	Tr, Tf	10			ps	
DC common mode voltage		-350		2850	mV	

Notes:

1 $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.1)}$$

where

f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

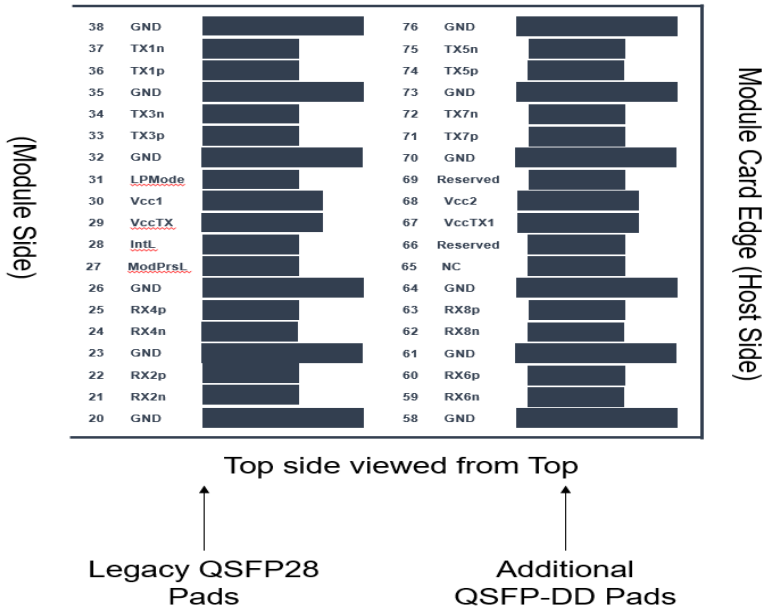
2 $$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \qquad \text{(Eq.2)}$$

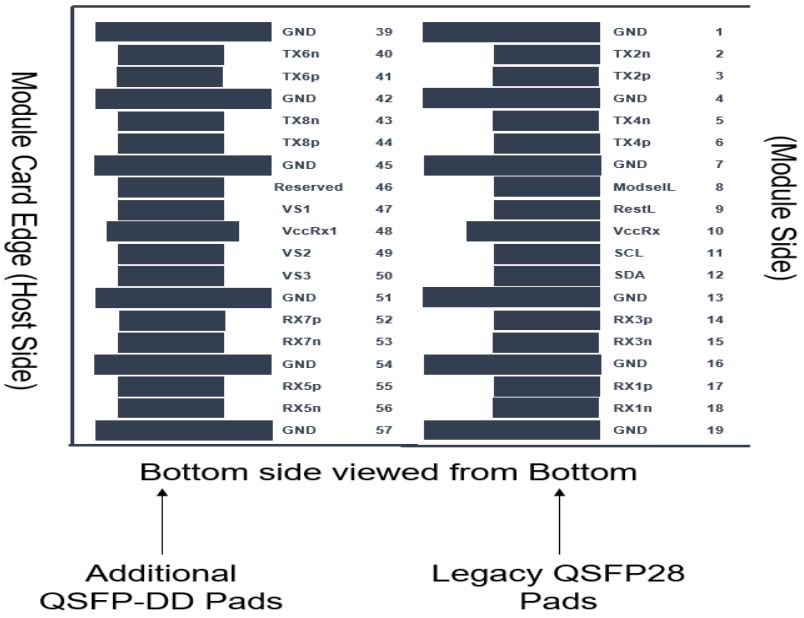
where f is the frequency in GHz,

RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

Pin Assignment

QSFP Module Pad Assignments and Descriptions





PIN	Symbol	Description	Notes
1	GND	Ground	1
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1

5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc RX	+3.3V Power Supply Receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc TX	+3.3V Power supply transmitter	2
30	Vcc1	+3.3V Power supply	2
31	LPMode	Low Power mode	
32	GND	Ground	1
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	TX1p	Transmitter Non-Inverted Data Input	

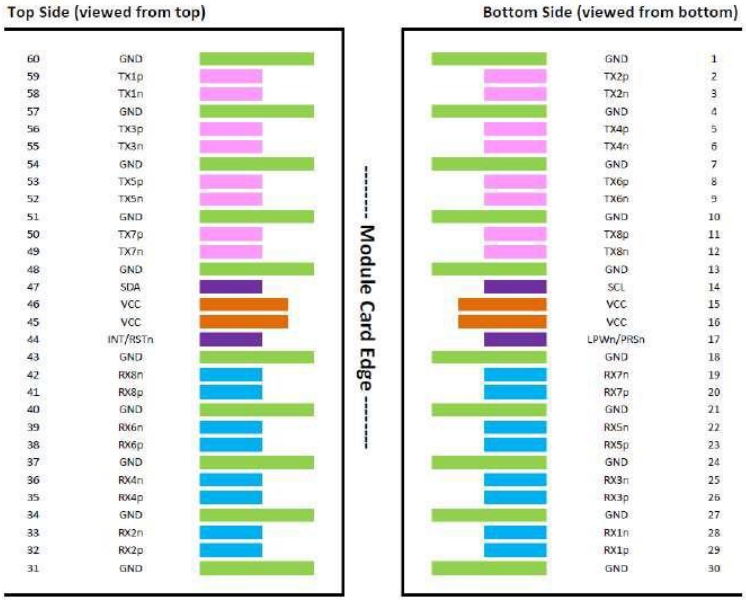
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	P/VS4	Module Vendor Specific 4	5
47	P/VS1	Module Vendor Specific 1	5
48	VCCRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	5
50	VS3	Module Vendor Specific 3	5
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For future use	3
67	VccTx1	3.3V Power Supply	2
68	Vcc2	3.3V Power Supply	2
69	ePPS/Clock	1PPS PTP clock or reference clock input	6

70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.
3. Reserved and no Connect pads recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see MODULE PAD ASSIGNMENT) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.
5. Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ
6. ePPS/Clock if not used recommended to be terminated with 50Ω to ground on the host.

OSFP Module Pad Assignments and Descriptions

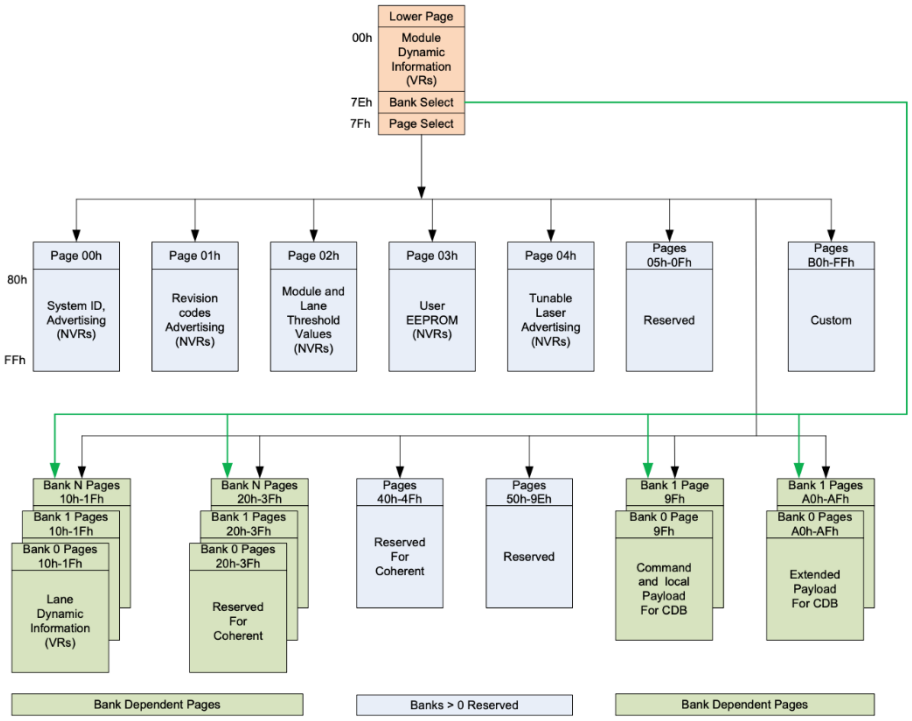


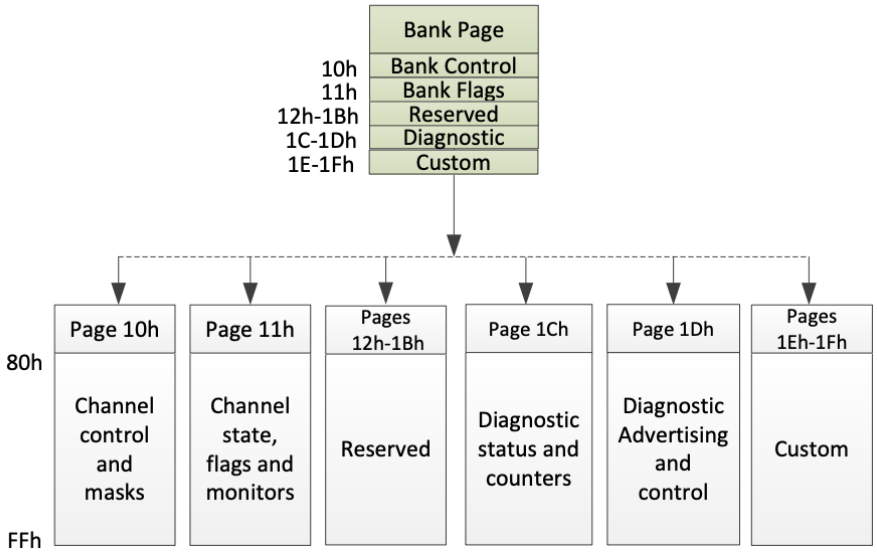
Pin	Symbol	Description	Plug Sequence
1	GND	Ground	1
2	Tx2p	Transmitter Data Non-Inverted	3
3	Tx2n	Transmitter Data Inverted	3
4	GND	Ground	1
5	Tx4p	Transmitter Data Non-Inverted	3
6	Tx4n	Transmitter Data Inverted	3
7	GND	Ground	1
8	Tx6p	Transmitter Data Non-Inverted	3
9	Tx6n	Transmitter Data Inverted	3
10	GND	Ground	1
11	Tx8p	Transmitter Data Non-Inverted	3
12	Tx8n	Transmitter Data Inverted	3
13	GND	Ground	1
14	SCL	2-wire serial interface clock	3
15	VCC	+3.3V Power	2
16	VCC	+3.3V Power	2
17	LPWn/PRSn	Low-Power Mode / Module Present	3
18	GND	Ground	1
19	Rx7n	Receiver Data Inverted	3
20	Rx7p	Receiver Data Non-Inverted	3
21	GND	Ground	1

22	Rx5n	Receiver Data Inverted	3
23	Rx5p	Receiver Data Non-Inverted	3
24	GND	Ground	1
25	Rx3n	Receiver Data Inverted	3
26	Rx3p	Receiver Data Non-Inverted	3
27	GND	Ground	1
28	Rx1n	Receiver Data Inverted	3
29	Rx1p	Receiver Data Non-Inverted	3
30	GND	Ground	1
31	GND	Ground	1
32	Rx2p	Receiver Data Non-Inverted	3
33	Rx2n	Receiver Data Inverted	3
34	GND	Ground	1
35	Rx4p	Receiver Data Non-Inverted	3
36	Rx4n	Receiver Data Inverted	3
37	GND	Ground	1
38	Rx6p	Receiver Data Non-Inverted	3
39	Rx6n	Receiver Data Inverted	3
40	GND	Ground	1
41	Rx8p	Receiver Data Non-Inverted	3
42	Rx8n	Receiver Data Inverted	3
43	GND	Ground	1
44	INT/RSTn	Module Interrupt / Module Reset	3
45	VCC	+3.3V Power	2
46	VCC	+3.3V Power	2
47	SDA	2-wire serial interface clock	3
48	GND	Ground	1
49	Tx7n	Transmitter Data Inverted	3
50	Tx7p	Transmitter Data Non-Inverted	3
51	GND	Ground	1
52	Tx5n	Transmitter Data Inverted	3
53	Tx5p	Transmitter Data Non-Inverted	3
54	GND	Ground	1
55	Tx3n	Transmitter Data Inverted	3
56	Tx3p	Transmitter Data Non-Inverted	3
57	GND	Ground	1

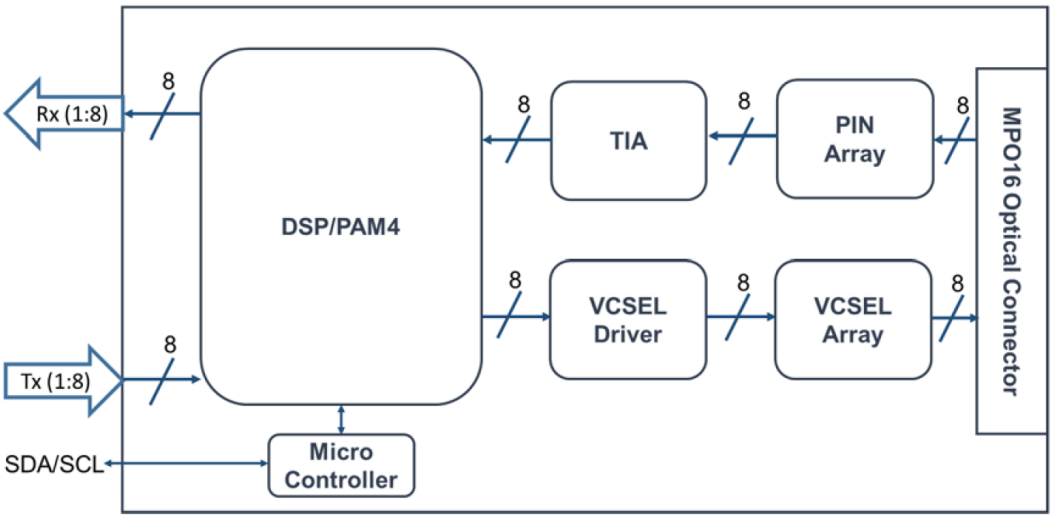
58	Tx1n	Transmitter Data Inverted	3
59	Tx1p	Transmitter Data Non-Inverted	3
60	GND	Ground	1

MEMORY MAP (compliant with CMIS 4.0)

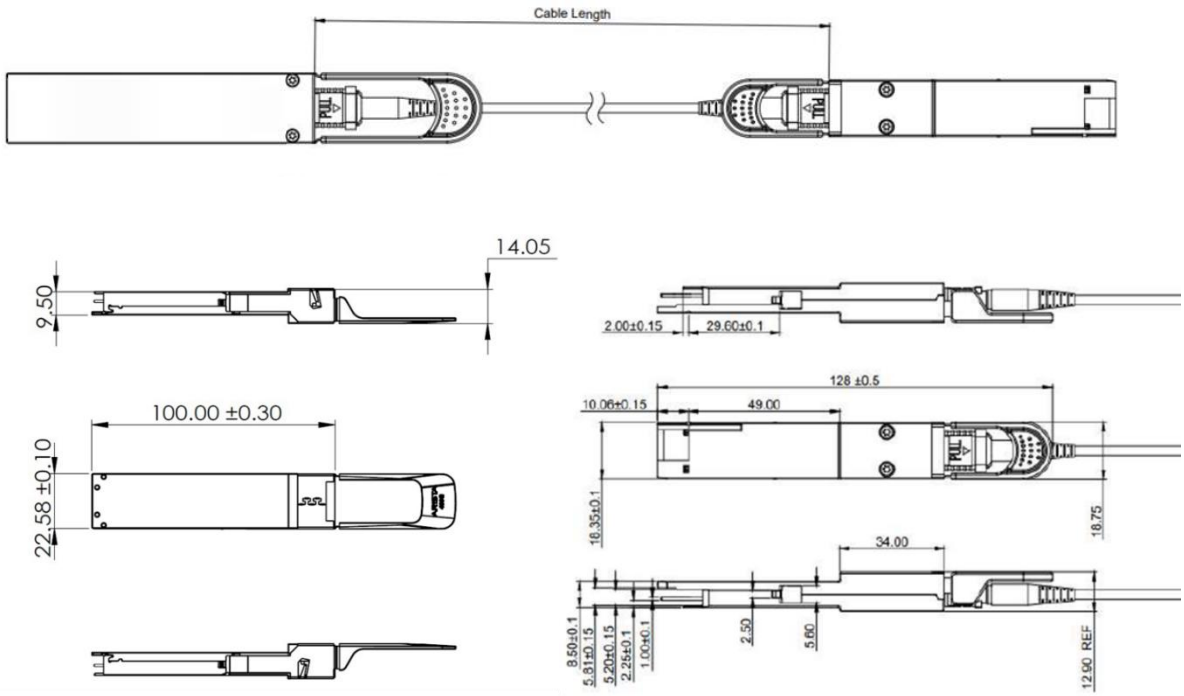




Recommended Host - Transceiver Interface Block Diagram



Mechanical Drawing



Ordering Information

Part No	Specification							
	Package	Data rate	Laser	Fiber	Cable Type	Cable Length	Temp.	Application
WS-D4O4-AOCLC034	QSFP-DD to OSFP(RHS)	400Gbps	850nm	OM4	LSZH	3m	0~70°C	400GbE InfiniBand SDR, QDR, DDR
WS-D4O4-AOCxCxx4	QSFP-DD to OSFP(RHS)	400Gbps	850nm	OM4	Ribbon LSZH OFNP, OFNR	xx	0~70°C	400GbE InfiniBand SDR, QDR, DDR

Note:

First x: Cable type: L for LSZH, P for OFNP, and R for OFNR

Length: xx

Modification History

Revision	Date	Description	Originator	Review	Approved
0.1	19-Jul-2023	New Issue	Shao Yu Lee	Tom Tang	Wayne Liao
0.2	19-Feb-2024	Update format	Joanne Ni	Ken Cheng	Tom Tang
0.3	27-Oct-2024	Update Power Consumption	Joanne Ni	Ken Cheng	Wayne Liao

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