Data Sheet

400G QSFP112 DR4 500m Transceiver Module
P/N: WST-Q112-DR4-C

Features:

- Supports 425Gb/s aggregate bit rate
- Hot Pluggable QSFP form factor
- 4x100G PAM4 EML/PIN photo detector
- Low Power Dissipation, Max. 13W
- Up to 500m transmission with SMF
- Single MPO12-APC receptacle
- Operating case temperature 0 to 70 ºC

Standards:

- SFF-8679: General Electrical
- IEEE 802.3bs: Physical Layer Specifications and Management Parameters
- CMIS 4.0 management interface

Applications:

- Ethernet for 400GBASE-DR4

General Product Characteristics

Parameter	Value	Unit	Comments
Module Form Factor	QSFP	As defined by QSFP112 MSA	Module Form Factor
Number of Lanes	4 TX and 4 RX		
Maximum Aggregate Data Rate	425	Gb/s	
Protocols Supported	Ethernet		
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by SFF-8679
Maximum Power Consumption	13	Watts	Varies with output voltage swing and pre-emphasis settings

Absolute Maximum Ratings

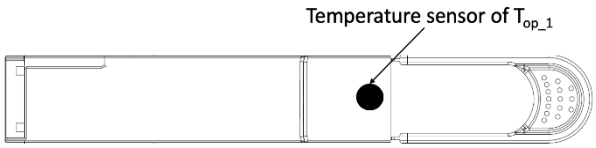
Exceeding the limits below may damage the active optical module permanently. Module performance is not guaranteed beyond the operating range.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Case Operating Temperature	T_{op_1}	0	60	°C	1, 2
	T_{op_2}	0	70	°C	2
Relative Humidity	RH	15	85	%	
Optical Receiver Input (each lane)			+5	dBm	

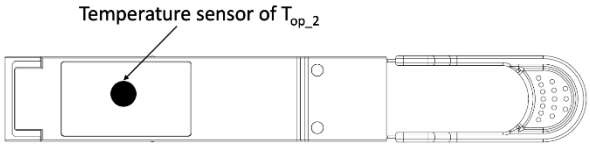
Notes:

1. DDMI temperature reading is measured by the position of Top_1
2. Case operating temperature definition:

Top view of module:



Bottom view of module:



Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		60	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Consumption	P_{Con}		10	13	W	
Bit Rate	BR		53.125		GBd	1
Pre-FEC Bit Error Ratio	BER			$2.4x10^{-4}$		2
Post-FEC Bit Error Ratio	BER			10^{-12}		
Transmit Distance	T_D	2		500	m	
Number of Lanes		4				
Logic Input Voltage High	V_{ih}	2		Vcc+0.3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Notes:

1. Single lane
2. PRBS13Q test pattern is used.

Electrical Characteristics

Parameter	Min	Typical	Max	Units	Notes
Transceiver Power Supply Current			4	A	
Transmitter at TP1a					
DC common-mode output voltage	-0.3		2.8	V	
Single-ended output voltage	-0.4		3.3	V	
AC common-mode RMS output voltage			25	mV	
Eye height	10			mV	
Vertical eye closure, VEC			12	dB	
Differential termination mismatch			10	%	
Differential peak-to-peak output voltage - Transmitter disabled			35	mV	
Differential peak-to-peak output voltage - Transmitter enabled			870	mV	
Common-mode to differential return loss	See Note 1				
Receiver at TP4					
AC common-mode output voltage			25	mV	
Differential peak-to-peak output voltage -short mode			600	mV	
Differential peak-to-peak output voltage -long mode			900	mV	
Eye Height	15			mV	
Differential termination mismatch	10			%	
Transition time (20% to 80%)	10			ps	
Common-mode to differential return loss	See Note 1				
DC common-mode voltage tolerance	-0.35		2.85	V	

Notes:

1. $$RLdc(f) \geq \begin{Bmatrix} 22 - 20\left(\frac{f}{53.125}\right) & 0.01 \leq f \leq 26.56 \\ 15 - 6\left(\frac{f}{53.125}\right) & 25.56 < f \leq 53.125 \end{Bmatrix} \text{ (dB)}$$

   where

   f is the frequency in GHz,

   RLdc is the common-mode to differential return loss in dB

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Signaling Speed per Lane		53.125±100ppm			GBd	
Lane Wavelength	λ	1304.5		1317.5	nm	
Average launch power, each lane	P_{avg}	-2.9		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	OMA_{outer}	-0.8		4.2	dBm	2
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			3.4	dBm	
Launch power in OMA_{outer} minus TDECQ, each lane		-2.2			dBm	
Extinction ratio	ER	3.5			dB	
Average launch power of OFF transmitter, each lane	P_{off}			-15	dBm	
Receiver						
Signaling Speed per Lane		53.125±100ppm			GBd	
Lane Wavelength	λ	1304.5		1317.5	nm	
Average receive power, each lane		-5.9		4	dBm	3
Receive Power, each lane	OMA_{outer}			4.2	dBm	4
Receiver Reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lanec (max)				-4.4	dBm	

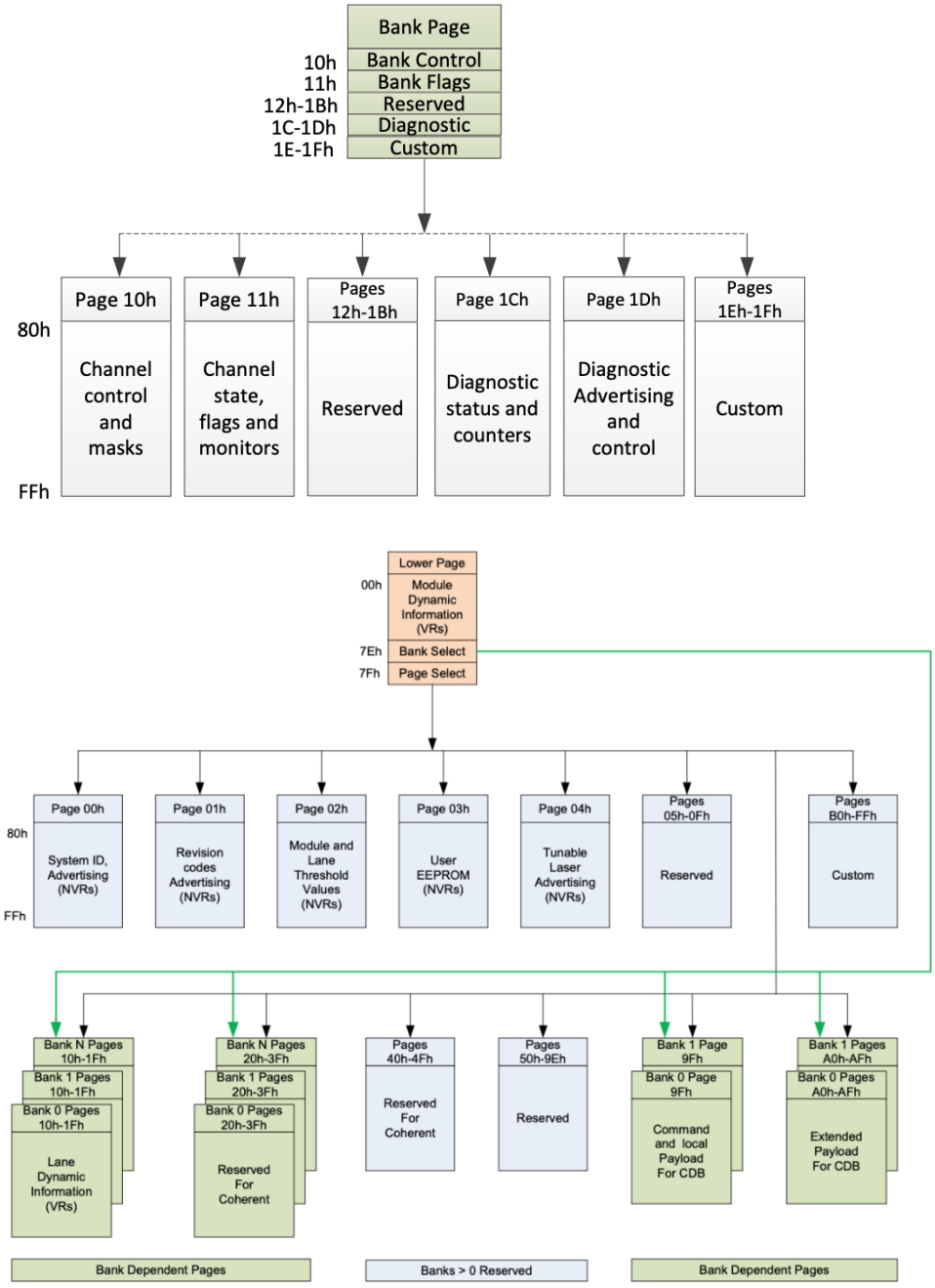
Notes:

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) must exceed these values.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal

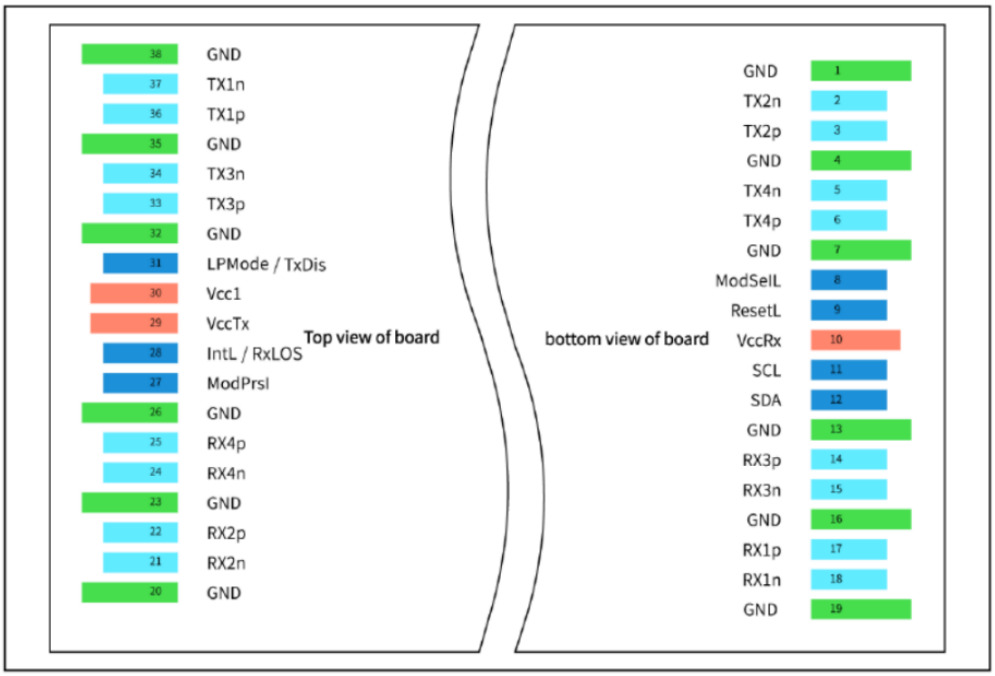
having this average power level. The receiver does not have to operate correctly at this input power.

4. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB

MEMORY MAP (compliant CMIS 4.0)



Pin Assignment (compliant SFF-8679)



PIN	Symbol	Description	Plug Sequence	Notes
1	GND	Ground	1	①
2	TX2n	Transmitter Inverted Data Input	3	
3	TX2p	Transmitter Non-Inverted Data Input	3	
4	GND	Ground	1	①
5	TX4n	Transmitter Inverted Data Input	3	
6	TX4p	Transmitter Non-Inverted Data Input	3	
7	GND	Ground	1	①
8	ModSelL	Module Select	3	②
9	ResetL	Module Reset	3	②
10	V_{cc} RX	+3.3V Receiver Power Supply Receiver	2	
11	SCL	2-wire Serial Interface Clock	3	
12	SDA	2-wire Serial Interface Data	3	

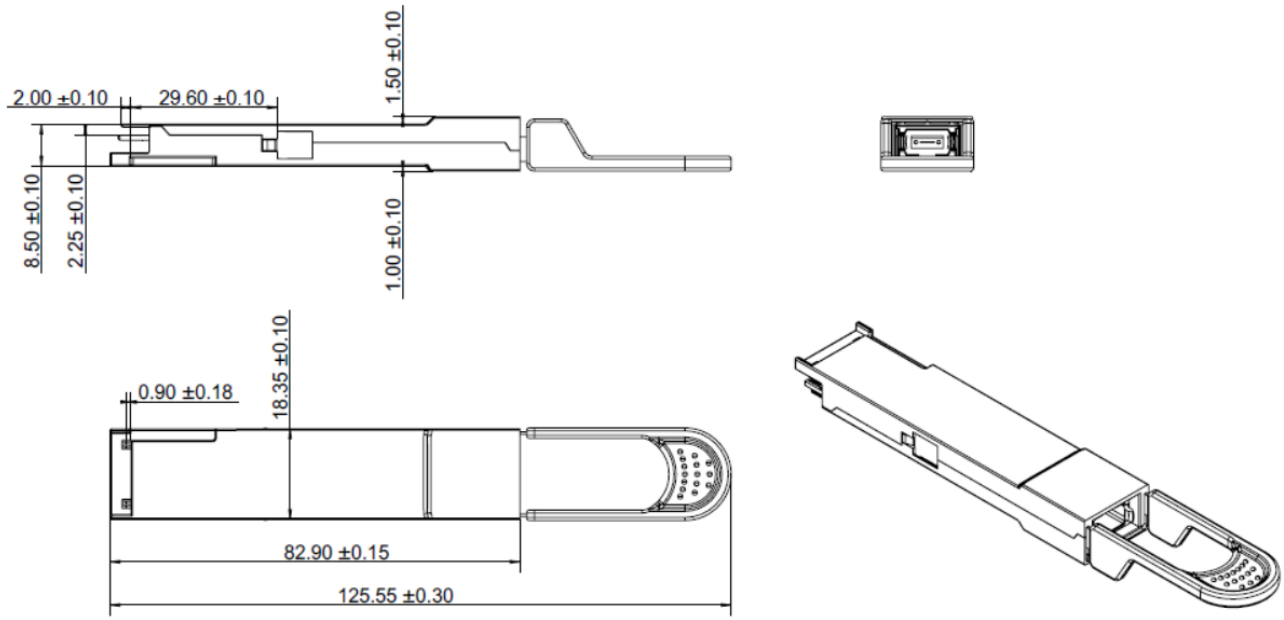
13	GND	Ground	1	1
14	RX3p	Receiver Non-Inverted Data Output	3	
15	RX3n	Receiver Inverted Data Output	3	
16	GND	Ground	1	1
17	RX1p	Receiver Non-Inverted Data Output	3	
18	RX1n	Receiver Inverted Data Output	3	
19	GND	Ground	1	1
20	GND	Ground	1	1
21	RX2n	Receiver Inverted Data Output	3	
22	RX2p	Receiver Non-Inverted Data Output	3	
23	GND	Ground	1	1
24	RX4n	Receiver Inverted Data Output	3	
25	RX4p	Receiver Non-Inverted Data Output	3	
26	GND	Ground	1	1
27	ModPrsL	Module Present, internal pulled down to GND	3	
28	IntL/RxLOS	Interrupt / optional RxLOS	3	
29	Vcc TX	+3.3V Transmitter Power Supply	2	2
30	Vcc1	+3.3V Power Supply	2	2
31	LPMode/TxDis	Low Power Mode / optional Tx Disable	3	
32	GND	Ground	1	
33	TX3p	Transmitter Non-Inverted Data Input	3	
34	TX3n	Transmitter Inverted Data Input	3	
35	GND	Ground	1	
36	TX1p	Transmitter Non-Inverted Data Input	3	
37	TX1n	Transmitter Inverted Data Input	3	
38	GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-Q112-DR4-D	QSFP112	53.125Gbd (PAM4) per channel	1310nm EML	-2.9~ +4.0 dBm each Channel	PIN	-4.4 dBm each Channel	0~70°C	500m	DDM RoHS	400G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	16-May-2024	New Release	Joanne Ni	Ken Cheng	Wayne Liao
V1.1	9-Aug-2024	Update the operating temp from D to C	Joanne Ni	Ken Cheng	Wayne Liao

Headquarters
16F-5, No. 75, Sec. 1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22101, Taiwan
Tel: +886-2-2698-7208
Fax: +886-2-2698-7210
Email: sales@wavesplitter.com
Website: https://wavesplitter.com/