WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G OSFP-RHS SR8 Optical Transceiver Module
P/N: WST-OR4-SR8-C

Features:

- Supports 425Gb/s aggregate bit
- 8x50G PAM4 VCSEL/PIN photo detector
- OSFP RHS form factor
- Power consumption: 9W Max
- Single MMF MPO-16/APC optical connector
- Hot Pluggable module
- 3.3V power supply
- 100m max reach with MMF OM4
- 70m max reach with MMF OM3
- Operating Case Temperature: 0℃~70℃

Applications:

- Ethernet for 400GBASE-SR8
- HPC Interconnects
- Proprietary Interconnections

Standard:

- CMIS Rev. 4.0 Management Interface
- Compliant to OSFP MSA Rev. 5.0
- OSFP-RHS mechanical spec
- SFF-8679: General Electrical
- IEEE 802.3cd: Physical Layer Specifications and Management Parameters
- Compliant to Class 1 Laser Safety
- RoHS2.0 Compliance

Absolute Maximum Ratings

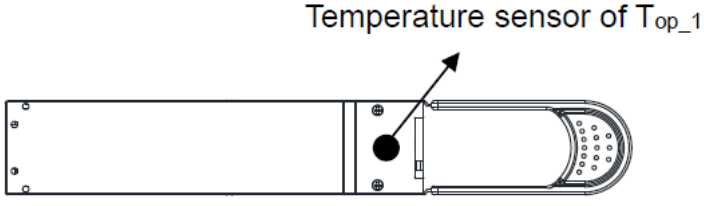
Exceeding the limits below may damage the module permanently.

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Note
Storage Temperature	T_S	-40		85	℃	
Case Operating Temperature	T_{op_1}	0		70	℃	1
Supply Voltage	VCC	-0.5		3.6	V	
Relative Humidity	RH	5		70	%	
Damage threshold, each lane		5			dBm	

Notes:

1. DDMI temperature reading is measured by the position of Top_1

Top view of module:



General Product Characteristics

Parameter	Value	Unit	Comments
Module Form Factor	OSFP	As defined by OSFP Rev 2.0	RHS form factor with MPO optical interface
Number of Optical Lanes	8 TX and 8 RX		
Maximum Aggregate Data Rate	425	Gb/s	26.5625Gbd PAM4 mode
Protocols Supported	Ethernet		
Electrical Interface and Pinout	60-pin edge connector		Pin-out as defined by OSFP Rev 5.0
Maximum Power Consumption	9	Watts	8 lanes operation, mission mode
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by CMIS Rev. 4.0

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Case Temperature	TOP	0		70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Maximum Power Consumption	P_{Con}			9	Watts	
Bit Rate	BR		26.5625		GBd	
Number of Lanes	-	8				
Pre-FEC Bit Error Ratio	BER			$2.4x10^{-4}$		1
Management Interface		Serial, I2C-based, maximum frequency 400 kHz				2
Logic Input Voltage High	V_{ih}	2		Vcc+3	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Notes:

1. PRBS31Q test pattern is used.
2. As defined by CMIS Rev. 4.0

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transmitter electrical input characteristics at TP1a					
AC common-mode output voltage(RMS)			17.5	mV	1
Differential peak-to-peak output voltage (Transmitter disabled)			35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)			880	mV	
Eye symmetry mask width		0.22		UI	
Eye height, differential	32			mV	
Differential output return loss	See Eq. 1				
Common to differential mode conversion return loss	See Eq. 2				
Differential termination mismatch	10			%	
Transition time (20% to 80%)			10	ps	
Receiver electrical output characteristics at TP4					
Far-end Eye height, differential	30			mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	See Eq. 1				
Common to differential mode conversion return loss	See Eq. 2				
Differential termination mismatch	10			%	
Transition time (20% to 80%)	10			ps	
DC common mode voltage	-350		2850	mV	

Note:

1. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(Eq.1)}$$

   where

   f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

2. $$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(Eq.2)}$$

   where *f* is the frequency in GHz,

   RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter						
Signaling rate, each lane (range)		26.5625±100 ppm			GBd	
Lane Wavelength	λ	840		868	nm	
RMS spectral width				0.6	nm	
Average launch power, each lane	P_{avg}	-6.5		4	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane (max)		-4.5		3	dBm	2
Transmit OMA per Lane	OMA	-6.4		3	dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	TDEC			4.5	dBm	
Launch power in OMAouter minus TDECQ (min)		-5.9			dBm	
Extinction ratio, each lane	ER	3			dB	
Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Receiver						
Signaling Speed per Lane		26.5625±100ppm			Gb/s	
Lane wavelengths (Range)	λ	840		868	nm	
Damage threshold, each lane		5			dBm	
Average receive power, each lane		-8.4		4	dBm	1
Received power (OMA), each lane				3	dBm	
Receiver Reflectance				-12	dB	
Receiver sensitivity in OMAouter				-7	dBm	2

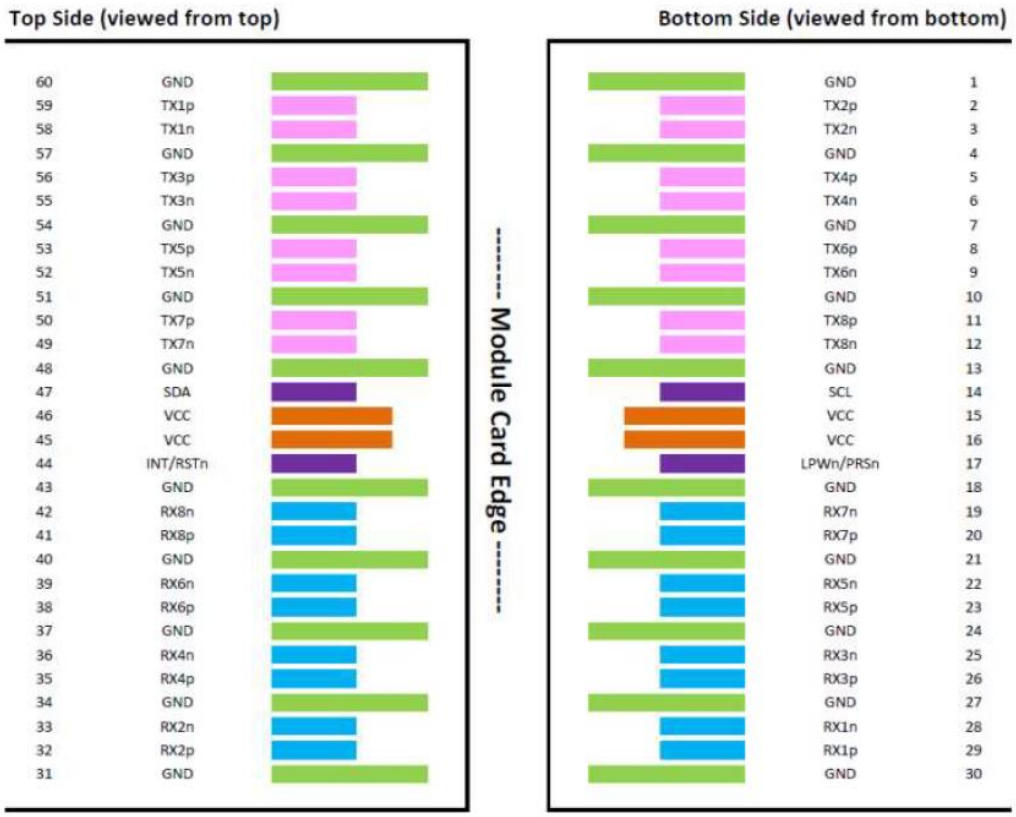
Notes:

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
2. Receiver sensitivity is informative and is defined for a transmitter with SECQ = 0.9 dB.

Module Electrical Connector

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram below. It provides 16 contacts of 8 differential pairs of high-speed transmit signals, 16 contacts of 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.



PIN Descriptions (compliant with OSFP MSA Rev 5.0)

Name	Direction	Description
TX[8:1]p	Input	Transmit differential pairs from host to module
TX[8:1]n	Input	
RX[8:1]p	Output	Receiver differential pairs from module to host.
RX[8:1]n	Output	
SCL	bidir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

LPWn/PRSn	bidir	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in Section 10.5.3
INT/RSTn	bidir	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in Section 10.5.2
VCC	Power	3.3V power for module
GND	ground	Module Ground. Logic and power return path.

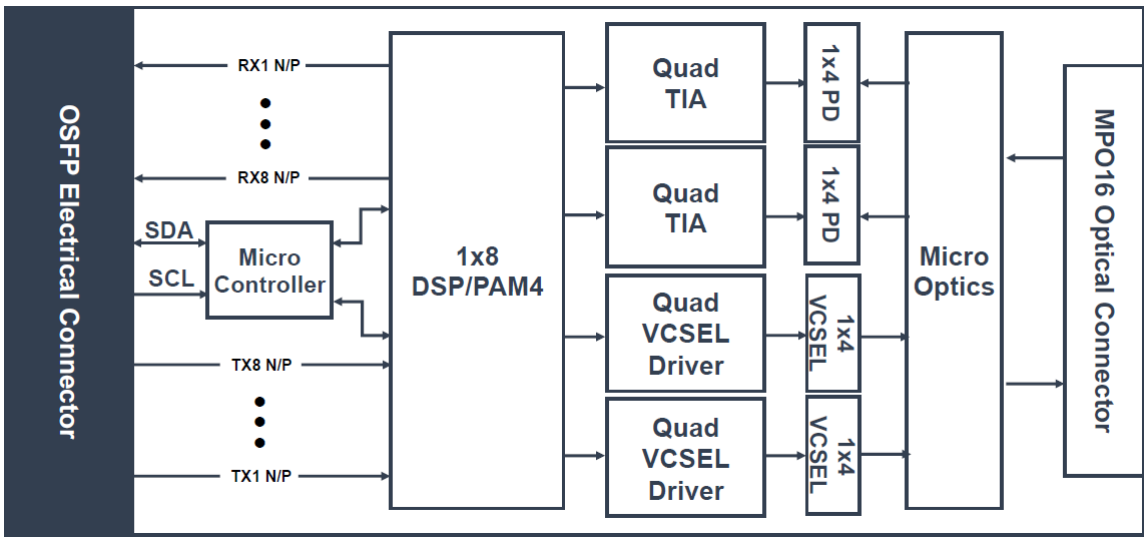
PIN List

PIN	Symbol	Description	Direction	Note
1	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	Input from Host	
3	TX2n	Transmitter Data Inverted	Input from Host	
4	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	Input from Host	
6	TX4n	Transmitter Data Inverted	Input from Host	
7	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	Input from Host	
9	TX6n	Transmitter Data Inverted	Input from Host	
10	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	Input from Host	
12	TX8n	Transmitter Data Inverted	Input from Host	
13	GND	Ground		
14	SCL	2-wire Serial interface clock	Bi-directional	Open-Drain with pull-up resistor on host
15	VCC	+3.3V Power supply	Power from Host	
16	VCC	+3.3V Power supply	Power from Host	
17	LPWn/PRSn	Low-Power Mode / Module Present	Bi-directional	Open-Drain with pull-up resistor on host
18	GND	Ground		

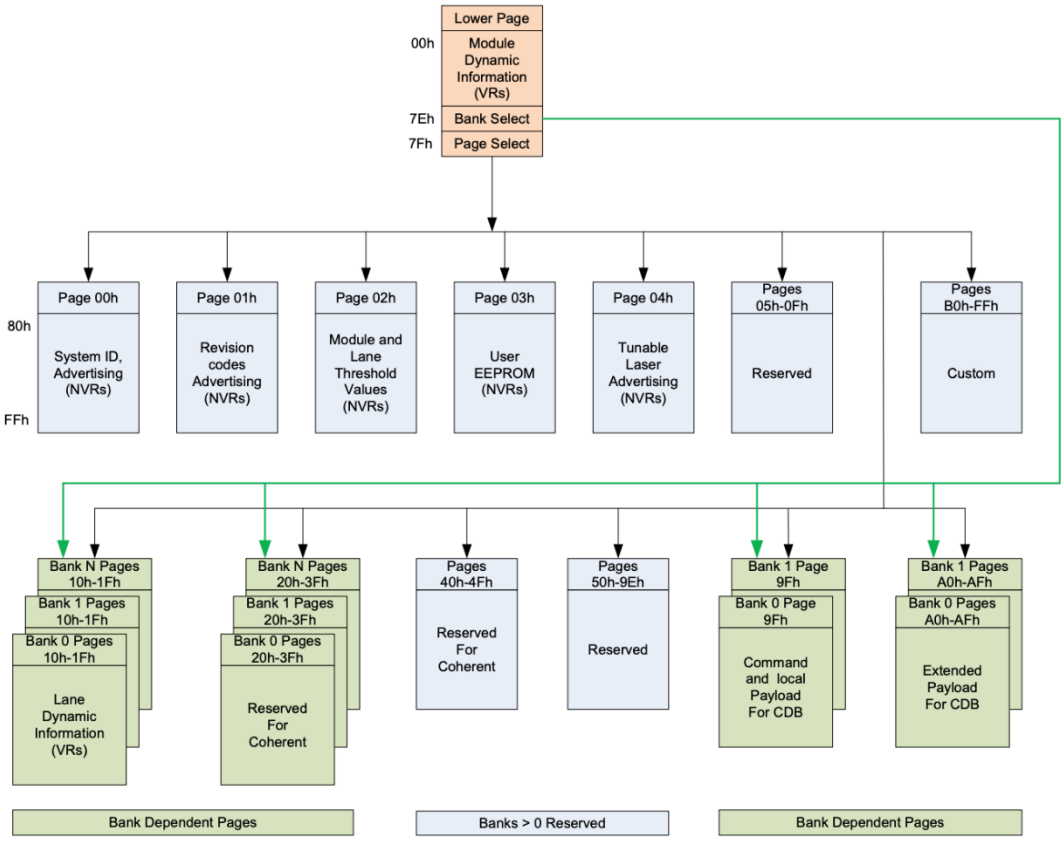
19	RX7n	Receiver Data Inverted	Output to Host	
20	RX7p	Receiver Data Non-Inverted	Output to Host	
21	GND	Ground		
22	RX5n	Receiver Data Inverted	Output to Host	
23	RX5p	Receiver Data Non-Inverted	Output to Host	
24	GND	Ground		
25	RX3n	Receiver Data Inverted	Output to Host	
26	RX3p	Receiver Data Non-Inverted	Output to Host	
27	GND	Ground		
28	RX1n	Receiver Data Inverted	Output to Host	
29	RX1p	Receiver Data Non-Inverted	Output to Host	
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	Output to Host	
33	RX2n	Receiver Data Inverted	Output to Host	
34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	Output to Host	
36	RX4n	Receiver Data Inverted	Output to Host	
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	Output to Host	
39	RX6n	Receiver Data Inverted	Output to Host	
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	Output to Host	
42	RX8n	Receiver Data Inverted	Output to Host	
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Bi-directional	See pin description for required circuit
45	VCC	+3.3V Power supply	Power from Host	
46	VCC	+3.3V Power supply	Power from Host	

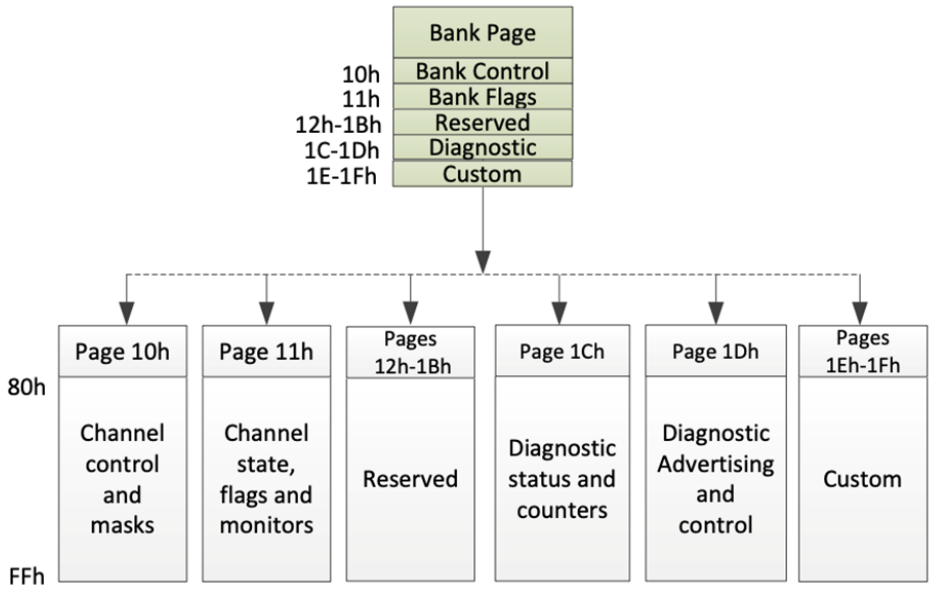
47	SDA	2-wire Serial interface data	Bi-directional	Open-Drain with pull-up resistor on HOST
48	GND	Ground		
49	TX7n	Transmitter Data Non-Inverted	Input from Host	
50	TX7p	Transmitter Data Inverted	Input from Host	
51	GND	Ground		
52	TX5n	Transmitter Data Non-Inverted	Input from Host	
53	TX5p	Transmitter Data Inverted	Input from Host	
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	Input from Host	
56	TX3p	Transmitter Data Non-Inverted	Input from Host	
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	Input from Host	
59	TX1p	Transmitter Data Non-Inverted	Input from Host	
60	GND	Ground		

Transceiver Block Diagram



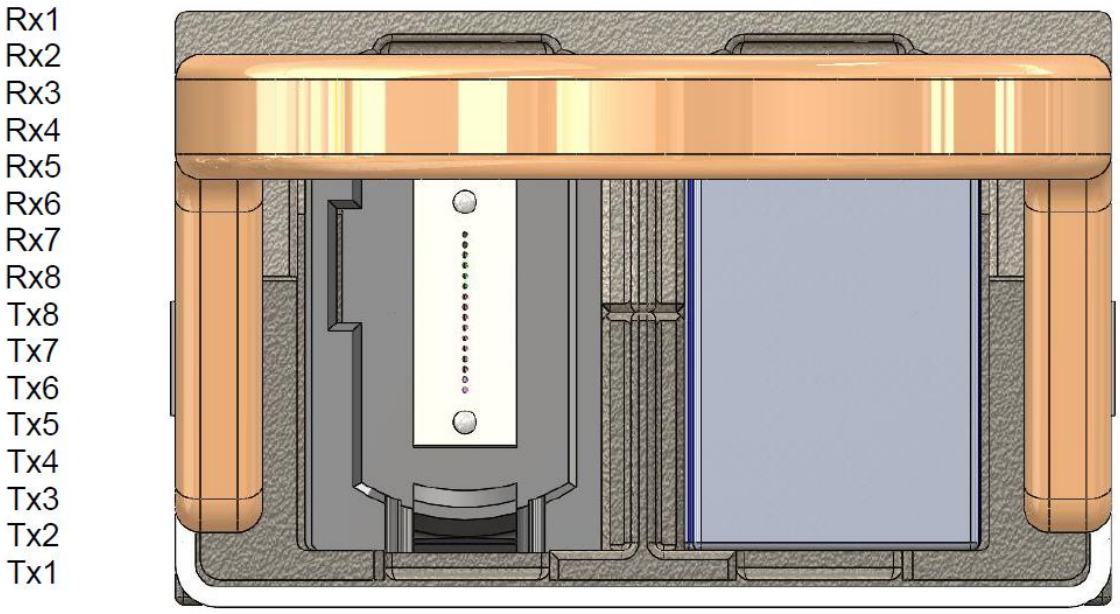
Memory Map ((compliant with CMIS Rev. 4.0))

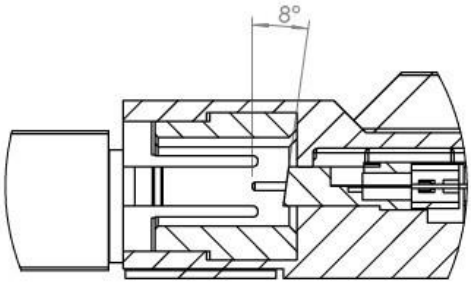


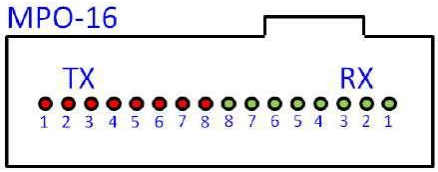


Transceiver Optical MPO Connectors

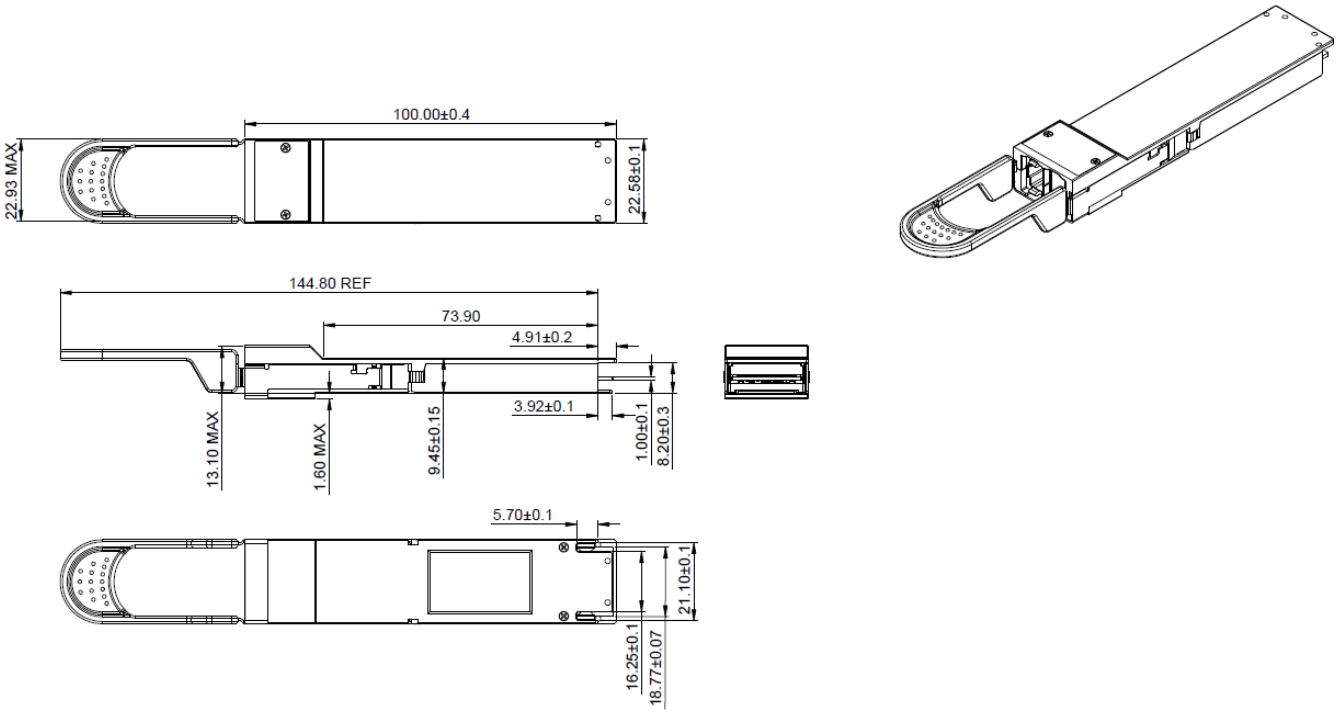
Below picture shows channel orientation of the optical connector when MPO16 connectors are used in an OSFP module. MPO16 connectors, which channel assignment within the connector to be as in the below picture.







Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-OR4-SR8-C	OSFP RHS	26.5625 Gbd each Channel	850nm VCSEL	-6.5~+4 dBm each Channel	PIN	< -7	0~70°C	OM3 70m OM4 100m	DDM RoHS	400G Ethernet

Note: Receiver sensitivity is informative and is defined for a transmitter with SECQ = 0.9 dB.

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	08-Aug-2024	New Release	Joanne Ni	Ken Cheng	Wayne Liao

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